ATOMIC LAYER DEPOSITION Al_2O_3-PASSIVATED AlGaN/GaN HIGH-ELECTRON-MOBILITY TRANSISTORS ON Si(111) TOWARDS RELIABLE HIGH-SPEED ELECTRONICS

BY

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DISSERTATION

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Professor Elyse Rosenbaum

ABSTRACT

(Al)GaN-based transistors are the backbones of next-generation high power/frequency electronics. However, various challenges with this exciting technology still necessitate more comprehensive investigations. In particular, epitaxially growing high-quality (Al)GaN layers on foreign substrates, forming low-resistance ohmic contacts on (Al)GaN materials, properly passivating (Al)GaN surfaces, and reducing leakage currents are of great importance. In this dissertation, these challenges are individually addressed along with respective detailed studies.

It is shown that a low GaN in-plane tensile strain allows a higher 2D electron gas mobility due to the alleviated interface roughness scattering. In addition, an ohmic contact specific resistance of 4×10^{-6} Ω–cm^2 with Ti/Al/Ni/Au metal stacks has been achieved by three-step rapid thermal annealing. Furthermore, it is revealed that annealed, thin-Al_2O_3 dielectric is an effective (Al)GaN surface passivation alternative for minimizing passivation-associated parasitic capacitance, yet non-ideal for significantly suppressing gate leakage current in metal-insulator-semiconductor structures due to the governing trap-assisted tunneling carrier transport mechanism. A 3.5 μm Schottky-gate AlGaN/GaN HEMT with V_T and g_m of -0.87 V and 131.67 mS/mm, respectively, at V_{DS} = 3.5 V has been demonstrated. The measured high Schottky gate leakage current and OFF-state drain current are believed to be responsible for the large subthreshold swing and low drain current on/off ratio. A passivation-last process followed by post-metallization annealing is then utilized, which largely reduces the reverse biased Schottky-gate leakage current and OFF-state drain current, leading to a low subthreshold swing of 84.75 mV/dec and a high drain current on/off ratio of 2.1×10^7. Together, the presented results add constructive inputs to the realization of reliable AlGaN/GaN HEMTs on Si(111) towards reliable high-speed electronics.

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Throughout my doctorate, I performed research on AlGaN/GaN high-electron-mobility transistors towards reliable high-speed electronics in the Innovative COmpound semiconductoR LABoratory (ICORLAB) led by Prof. Can Bayram. I practically designed unique sets of photomasks as well as process flow and performed hands-on device microfabrication and measurements using the advanced facilities in the Holonyak Micro and Nanotechnology Laboratory and Frederick Seitz Materials Research Laboratory at the University of Illinois at Urbana-Champaign. It has been a challenging and rewarding journey. I was given an incredible opportunity to self-develop in an environment full of clever minds at one of the most prestigious institutions in the world, and all of this was made possible by my advisor, Prof. Can Bayram.

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I dedicate this dissertation to my family for the unconditional love and support in my life.

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CHAPTER 1 MOTIVATION FOR HIGH-SPEED ELECTRONICS

In the past several decades, telecommunication technology has evolved progressively (Figure 1.1, [1]), and the fifth-generation (5G) wireless system is expected to be commercially launched in the year 2020 in order to cope with the rapid growth of number of mobile devices on the globe and new emerging wireless applications such as Internet of things (IoTs), autonomous cars, and high-definition (HD) video steaming. Compared to the previous generations, 5G is to be backed by millimeter wave transmission, massive MIMO (multiple-input, multiple-output), beamforming, and full duplex, aiming at supporting frequency band of 30 ~ 300 GHz, bandwidth of 400 MHz, peak data rate of 20 Gbps, and latency less than 1 ms, and area traffic capacity of 10 Mbps/m^2, as shown in Figure 1.2 However, due to the shorter wavelength that leads to worse propagation loss, the millimeter waves cannot easily travel through buildings or obstacles and can also be easily absorbed by rain and foliage. As a result, in cities, for example, dense networks of small cells populated every 250 meters have to be established in order to support such a high-speed infrastructure [2]. As such, the embedded semiconductor devices that power the 5G cells have to possess high operation frequency, high power, and most importantly, high power density.

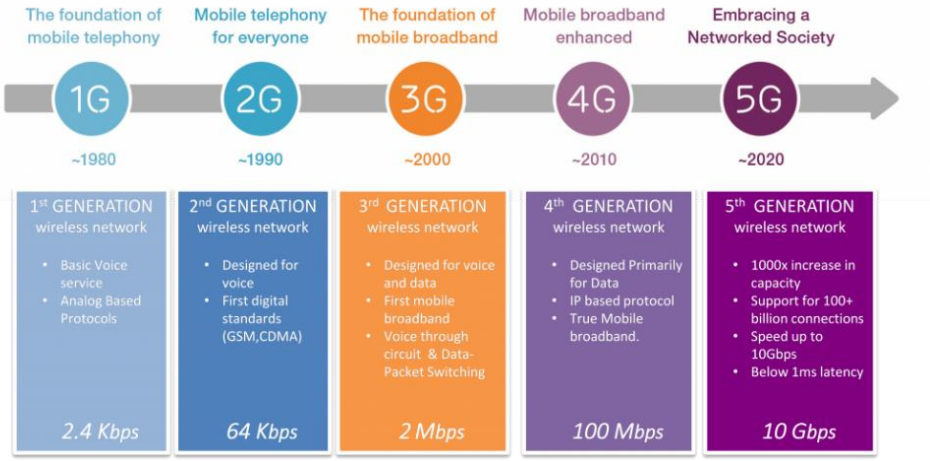

Figure 1.1. Evolution of telecommunication technology. © Ericsson. Reprinted from [1].

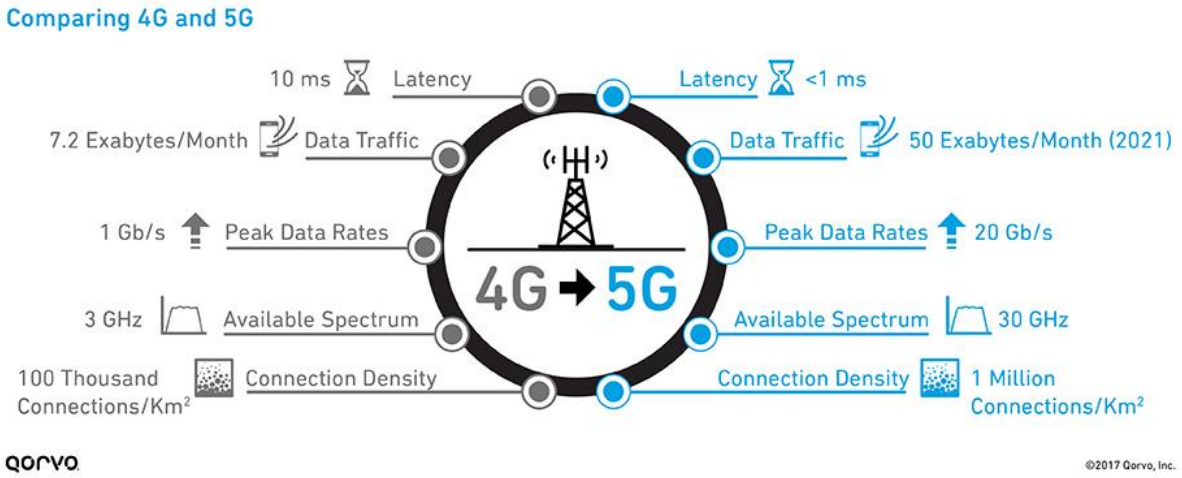

Figure 1.2. Comparison of 4G and 5G. © 2017 Qorvo, Inc. Reprinted from [3].

Gallium nitride (GaN) is a compound semiconductor that is of great interest for high-power and high-frequency applications due to its superior material properties. Compared with several conventional semiconductors as shown in Table 1.1, GaN is a semi-ionic crystal with a large bandgap, leading to high breakdown electric field that allows high device power density. In addition, the unique III-nitride material polarization allows the formation of high-electron-mobility transistor (HEMT) structures with high 2-D electron gas (2DEG) concentration and mobility but without the need for a doped barrier layer. Furthermore, GaN has inherently high electron saturation velocity and high chemical and thermal stability [4]. All the aforementioned properties of GaN make it one of the most promising and suitable candidates for supporting 5G technology and beyond, as indicated in Figure 1.3.

Table 1.1. Comparison of semiconductor properties.

Properties	Si	GaAs	SiC	GaN (Wurzite)
Bandgap (eV)	1.10	1.42	3.26	3.4
Breakdown field (MV/cm)	0.3	0.4	3.0	3.3
Electron saturation velocity ($\times 10^7$ cm/s)	1.0	1.0	2.0	2.5
Bulk Intrinsic concentration (cm^{-3}) 2DEG sheet concentration (cm^{-2})	1.5×10^{10}	1.5×10^{6}	8.2×10^{-9}	Bulk: 2×10^{-10} 2DEG: 1×10^{13}
Electron mobility (cm^2/V-s)	1,350	8,500	700	Bulk: 1,200 2DEG: 2,000

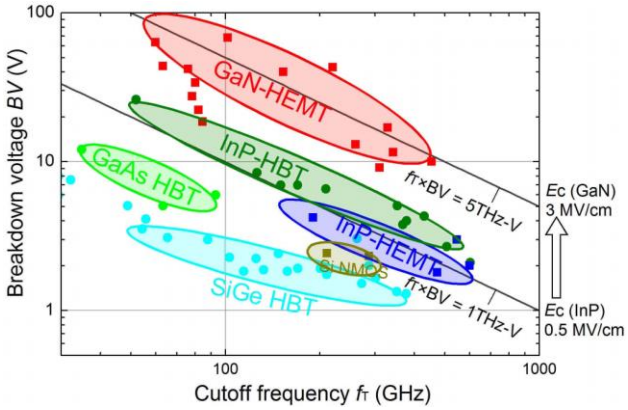

Figure 1.3. Power/frequency performance comparison among GaAs-, SiGe-, InP-, and GaN-based transistors. GaN HEMT shows promising potential in simultaneously achieving high power and high frequency. © IEEE 2013. Reprinted, with permission, from [5].

However, there are yet challenges faced by such exciting technology, including scalable high-quality epitaxial crystal growth, low-resistance ohmic contact formation, proper (Al)GaN surface passivation with low density of interface trap states, and low transistor gate leakage and OFF-state drain leakage. In this dissertation, these challenges are individually addressed along with respective studies of proposed solutions and their results, all together adding constructive inputs to the realization of reliable AlGaN/GaN HEMTs on Si(111) towards reliable high-speed electronics.

In Chapter 2, theories regarding AlGaN/GaN HEMTs are introduced, including the material polarizations, the formation of 2DEG, and material stack energy band diagram. In addition, basic transistor structure is shown along with the equivalent circuit model, followed by introductions of several key aspects for realizing reliable high-speed AlGaN/GaN HEMTs.

In Chapter 3, AlGaN/GaN high-electron-mobility transistor (HEMT) structures are grown on 200-mm diameter Si(111) substrates by using three different buffer layer configurations: (a) thick-GaN / 3 × {$Al_xGa_{1-x}N$} / AlN, (b) thin-GaN / 3 × {$Al_xGa_{1-x}N$} / AlN, and (c) thin-GaN / AlN, so as to have crack-free and low-bow (< 50 μm) wafer. Scanning electron microscopy, energy-dispersive X-ray spectroscopy, high-resolution cross-section transmission electron microscopy, optical microscopy, atomic-force microscopy, cathodoluminescence, Raman spectroscopy, X-ray diffraction ($\omega/2\theta$ scan and symmetric/asymmetric ω scan (rocking curve scan), reciprocal space mapping) and Hall effect measurements are employed to study the structural, optical, and electrical properties of these AlGaN/GaN HEMT structures. The effects of buffer layer stacks (i.e. thickness and content) on defectivity, stress, and two-dimensional electron gas (2DEG) mobility and 2DEG concentration are reported. It is shown that 2DEG characteristics are heavily affected by the employed buffer layers between AlGaN/GaN HEMT structures and Si(111) substrates. Particularly, we report that in-plane stress in the GaN layer affects the 2DEG mobility and 2DEG carrier concentration significantly. Buffer layer engineering is shown to be essential for achieving high 2DEG mobility (> 1800 cm^2/V-s) and 2DEG carrier concentration (> 1.0×10^{13} cm^2) on Si(111) substrates.

In Chapter 4, the importance of forming low-resistance ohmic contacts is addressed, followed by the theory of forming ohmic contacts on n-type GaN materials using metal stacks of Ti/Al/Ni/Au with properly designed rapid thermal annealing (RTA) process. In addition, through

optimizing the RTA temperature profile, a specific contact resistance of 4.04×10^{-6} Ω-cm^2 and a contact resistance of 0.27 Ω–mm is achieved in this work. However, from the images taken by atomic force microscopy and scanning electron microscopy, it is shown that the annealed ohmic contact surface exhibits high roughness, which could potentially pose further challenges when it comes to reducing parasitic capacitance for high-speed applications.

In Chapter 5, annealed, thin(~ 2.6 nm)-Al_2O_3/AlGaN/GaN metal-insulator-semiconductor (MIS) heterostructures on Si(111) are fabricated and studied via capacitance–voltage (C–V) measurements to quantify densities of fast and slow interface trap states and via current–voltage (I–V) measurements to investigate dominant gate current leakage mechanisms. Dual-sweep C–V measurements reveal small voltage hysteresis (~ 1 mV) around threshold voltage, indicating a low slow interface trap state density of ~ 10^9 cm^{-2}. Frequency-dependent conductance measurements show fast interface trap state density ranging from 8×10^{12} to 5×10^{11} eV^{-1}cm^{-2} at energies from 0.275 to 0.408 eV below the GaN conduction band edge. Temperature-dependent I–V characterizations reveal that trap-assistant tunneling (TAT) dominates the reverse-bias carrier transport while the electric field across the Al_2O_3 ranges from 3.69 to 4.34 MV/cm, and the dominant Al_2O_3 trap state energy responsible for such carrier transport is identified as 2.13 ± 0.02 eV below the Al_2O_3 conduction band edge. X-ray photoelectron spectroscopy measurements on Al_2O_3 before and after annealing suggest an annealing-enabled reaction between Al-O bonds and inherent H atoms. Overall, we report that annealed, thin-Al_2O_3 dielectric is an effective (Al)GaN surface passivation alternative when minimizing passivation-associated parasitic capacitance is required, yet non-ideal for significantly suppressing gate leakage current in MIS structures due to the governing TAT carrier transport mechanism.

In Chapter 6, a normally-on 2 μm Schottky gate AlGaN/GaN high-electron-mobility transistor (HEMT) is fabricated and characterized. Due to the thin AlGaN barrier layer, the device has a high threshold voltage (V_T) of –0.87 V and therefore can be operated with a low supply voltage to reduce power consumption. $I_D - V_{DS}$ and $I_D - V_{GS}$ measurements reveal good pinch-off behavior and a $g_{m,max}$ of 131.67 mS/mm. In addition, drain current ON/OFF ratio ($I_{D,ON/OFF}$) and subthreshold swing (*S.S.*) are extracted as 3.6×10^4 and 170 mV/dec. Investigations of access (gate to drain and gate to source) and channel regions of the AlGaN/GaN HEMT are performed. Sheet resistance (R_S) in the access region is extracted as 476.62 ± 62.60 Ω/□. In addition, channel mobility increases from 240.23 to 509.66 cm^2/V-s with V_{GS} increasing from –0.2 to 0.4 V, suggesting that Coulomb scattering dominates in this bias range, presumably due to insufficient electrostatic screening. Temperature-dependent I–V measurements are also performed to reveal the effective Ni/GaN barrier height as a function of reverse-biased V_{GS}, where the presence of conductive leakage path due to dislocation-related continuum states is presumed to be responsible for the low effective barrier height (< 0.3 eV). The high reverse gate leakage current leads to high OFF-state drain current, which further causes the large *S.S.* and low $I_{D,ON/OFF}$.

In Chapter 7, Al_2O_3-passivated Schottky-gate AlGaN/GaN HEMTs with improved subthreshold swing and drain current on/off ratio by post-metallization annealing at 500 °C in N_2 ambient are reported. With the post-metallization annealing, the gate leakage current in the reverse biased region and off-state drain current are reduced by more than three orders of magnitude, leading to a low subthreshold swing of 84.75 mV/dec and a high drain current on/off ratio of 2.1×10^7. Through temperature dependent current-voltage measurements on dual Schottky gate structures and capacitance-voltage measurements on Al_2O_3/AlGaN/GaN MISHEMT capacitors, it is identified that the post-metallization annealing greatly suppresses both the Al_2O_3/AlGaN

interface leakage current and the reverse gate leakage current by eliminating Al_2O_3/AlGaN interface trap states with 0.34 eV trap state energy and changing the dominant mechanism of reverse gate leakage conduction from trap-assisted tunneling to Fowler–Nordheim tunneling, respectively. Overall, this work reports on the effectiveness of post-metallization annealing in improving the performance of Schottky-gate AlGaN/GaN HEMTs and the underlying improving mechanisms.

Chapter 8 summarizes the dissertation by emphasizing the conclusions and contributions of the work, followed by suggestions for future work in order to further mature the AlGaN/GaN HEMT technology towards reliable high-speed electronics.

CHAPTER 2 AlGaN/GaN HIGH-ELECTRON-MOBILITY TRANSISTORS (HEMTS)

2.1 Introduction to AlGaN/GaN HEMTs

Two-dimensional electron gas in the AlGaN/GaN-based heterostructure is formed due to the material polarization effects, including spontaneous polarization (P_{sp}) and piezoelectric polarization (P_{pe}). Spontaneous polarization exists in wurtzite-phase (Al)GaN materials due to the asymmetry of the crystal structure in the [0001] direction. Piezoelectric polarization is on the other hand induced by mechanical strain in the AlGaN layer due to the lattice constant mismatch in the AlGaN/GaN heterostructure. The discontinuity of the total polarization field across the heterojunction contributes to a fixed polarization charge (σ). Combining other factors including AlGaN thickness (d), surface donor state level (ϕ_B), conduction band offset (ΔE_C), and the Fermi level with respect to GaN-conduction-band-edge energy (E_F), the 2DEG sheet concentration (N_s) is expressed as

$$N_S(x) = \frac{\sigma(x)}{e} - \frac{\varepsilon_0 \varepsilon(x)}{de^2}\left[e\phi_B(x) + E_F(x) - \Delta E_C(x)\right] \tag{2.1}$$

$$\sigma = P_{SP}(\mathrm{AlGaN}) + P_{PE}(\mathrm{AlGaN}) - P_{SP}(\mathrm{GaN}) \tag{2.2}$$

$$P_{PE} = 2\frac{a - a_0}{a_0}\left(e_{31} - e_{33}\frac{C_{13}}{C_{33}}\right), \tag{2.3}$$

where x is the Al composition of the AlGaN layer, (a, a_0) are lattice constants for AlGaN and GaN, respectively. (C_{13}, C_{33}) are elastic constants and (e_{31}, e_{33}) are piezoelectric coefficients of the AlGaN layer (Figure 2.1) [6], [7], [8]. Using a self-consistent 1-dimensional Schrödinger–Poisson solver (*BandEng*), an AlGaN/GaN HEMT band diagram is simulated and shown in Figure 2.2.

The accumulated 2DEG in the triangular quantum well at the AlGaN/GaN heterojunction is in high concentration and is therefore suitable for high-electron-mobility transistors.

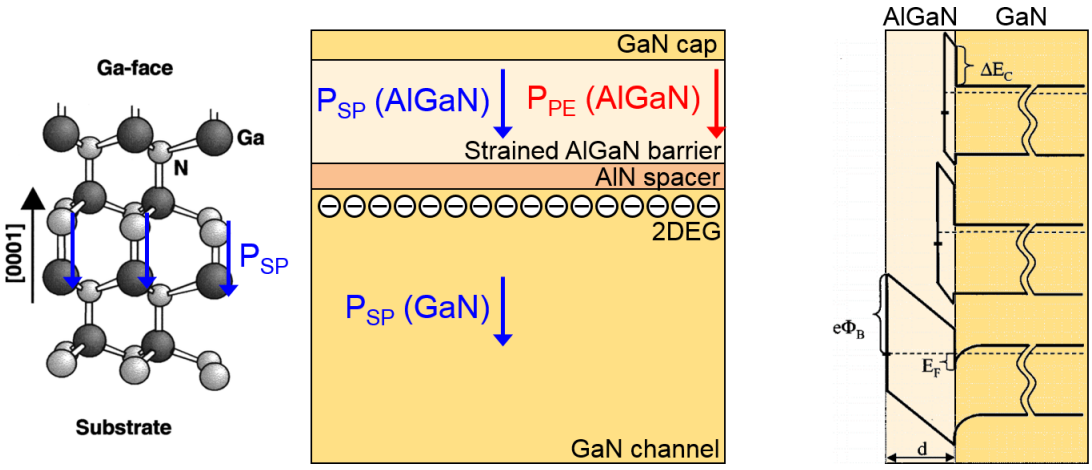

Figure 2.1. AlGaN/GaN heterostructure, polarizations, and 2DEG formation [6].

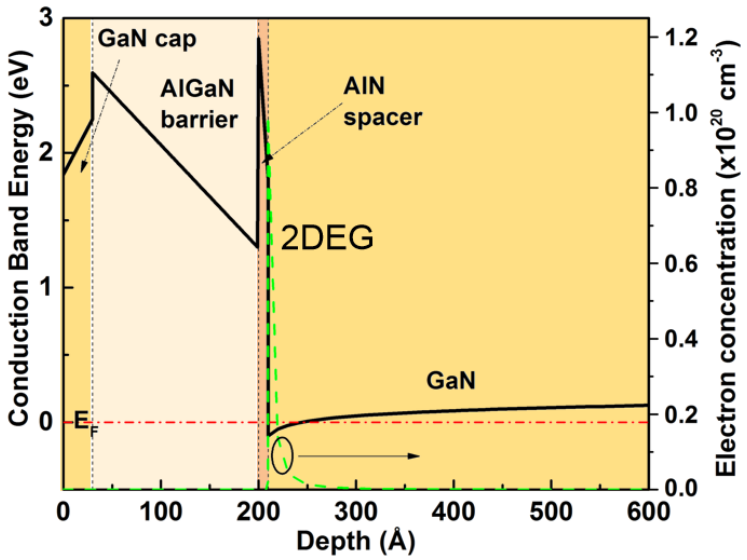

Figure 2.2. Simulated AlGaN/GaN HEMT band diagram.

AlGaN/GaN high-electron-mobility transistors (AlGaN/GaN HEMTs) have shown promising capabilities in enabling high-power/high-frequency operations and applications. Such

devices fall into the category of field effect transistors where output current is carried through a channel (either p-type or n-type) that has a conductivity that can be controlled by a transverse electric field provided by an applied external voltage bias. Rather than having a channel that is formed through the mechanism of inversion, the conductive channel of an AlGaN/GaN HEMT is inherently built due to polarizations that accumulate p-type or n-type carriers at the heterojunction of the material stack to form two-dimensional hole gas (2DHG) or two-dimensional electron gas (2DEG), respectively. Such a two-dimensional carrier gas that serves as a conductive channel can have a high carrier sheet concentration (~ 10^{13} cm^{-2} for 2DEG) and a high carrier mobility (~ 2,000 cm^2/V-s for 2DEG).

2.2 Small-signal equivalent circuit model

A schematic cross section image of an n-type AlGaN/GaN HEMT is shown in Figure 2.3; its high-frequency operation small-signal equivalent circuit model is illustrated in Figure 2.4.

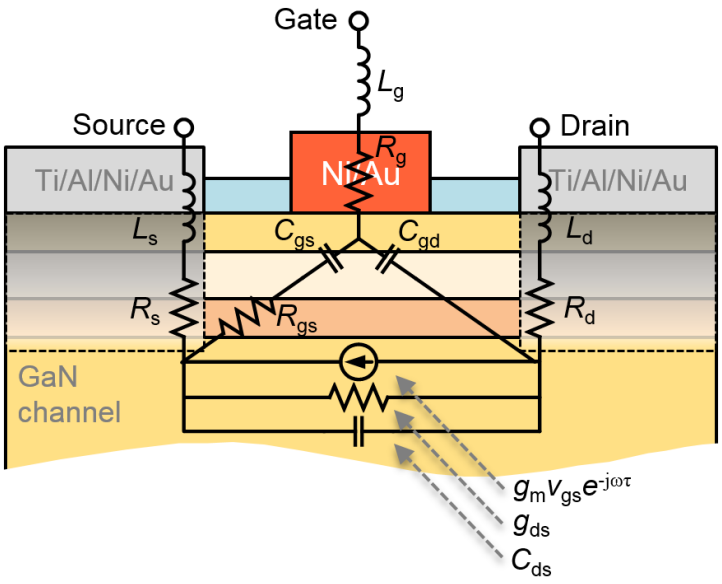

Figure 2.3. Schematic cross section of a GaN-on-Si high-electron-mobility transistor with the equivalent circuit components.

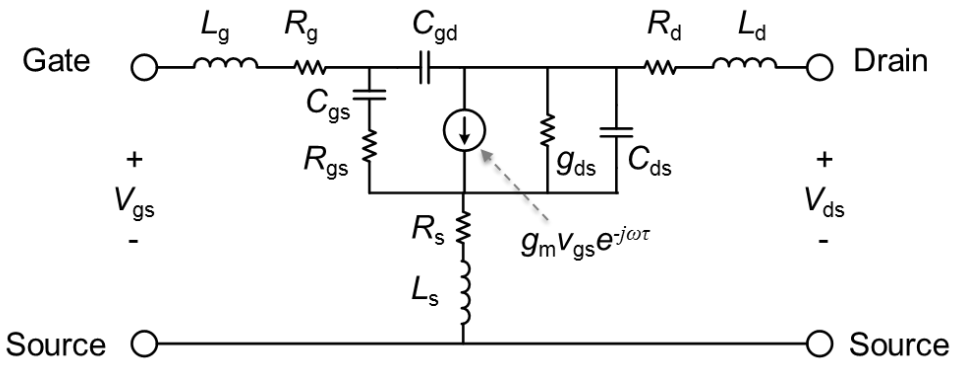

Figure 2.4. GaN-on-Si high-electron-mobility transistor high-frequency operation small-signal equivalent circuit model.

High-frequency operation performance of an individual device is commonly measured by its cutoff frequency (f_T); by definition, this quantity represents the frequency at which the magnification of short-circuit current gain becomes unity. The current state of the art for the f_T is 454 GHz coupled with a 10 V breakdown voltage [5]. Cutoff frequency is determined by various delay components, mainly including the intrinsic delay and the parasitic delay, shown as the following equation [9]:

$$f_T = \frac{1}{2\pi}\left\{\frac{\left(C_{gs}+C_{gd}\right)}{g_m} + C_{gd}\cdot\left(R_s+R_d\right)\cdot\left[1+\left(1+\frac{C_{gs}}{C_{gd}}\right)\frac{g_d}{g_m}\right]\right\}^{-1}. \quad (2.4)$$

The term $(C_{gs} + C_{gs})/g_m$ represents the intrinsic delay time, which has an equivalent form of $(L_g + \Delta L_g)/v_{avg}$, where L_g is the physical gate length, ΔL_g is the excess gate length due to drain depletion and gate fringing field, and v_{avg} is the average carrier (electrons or holes) velocity. Intuitively this quantity can be interpreted as how much time the carriers need to travel through the channel under the gate region. Both shrinking the gate length and increasing the average carrier velocity could

reduce the intrinsic delay time, which is also one of the main reasons that necessitates the device fabrication scaling technology. However, device scaling brings about issues of parasitic charging delay that is expressed by the other two terms in the equation. As can be seen in Figure 2.5, f_T starts to deviate from the ideal value that is solely decided by the intrinsic delay as the gate length is scaled below 100 nm.

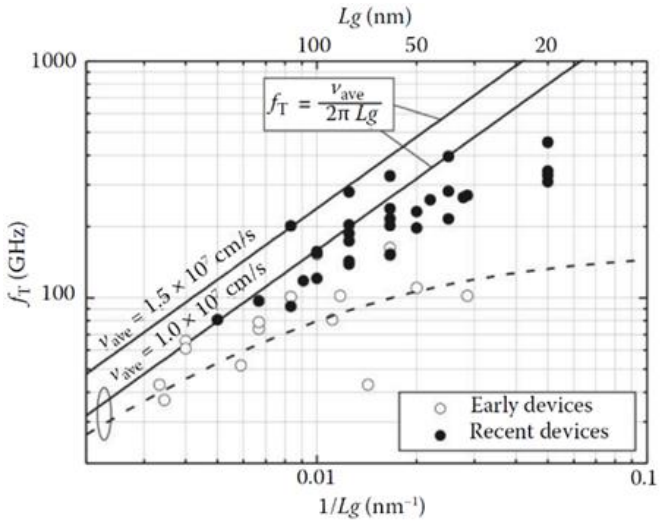

Figure 2.5. Cutoff frequency behavior with respect to gate length scaling [10].

The parasitic delay term $C_{gd} \cdot (R_s + R_d)$ represents the charging delay due to the source (S) and drain (D) resistance. Researches are still actively in progress to minimize these two resistances by optimizing the contact metal material stack [11] and introducing n^+ regions in between the S/D metal contacts and the channel region [5]. In addition, enlarging the physical distance from gate to drain is also beneficial in reducing the charging time since C_{gd} can therefore be reduced. Another advantage of enlarging the physical distance from gate to drain will be promoting the device breakdown voltage. The last term of the delay component comes from the existence of output conductance (g_d); it becomes more dominant when the gate length is further scaled down.

To ensure the horizontal scaling of the device will actually come into play as expected, vertical device scaling shall not be ignored. Researches have shown that in addition to the emerging of the parasitic delay, scaling the gate length will also induce short channel effect that severely compromises the device performance. Effects such as threshold voltage (V_{TH}) reduction, transconductance (g_m) reduction, increasing output conductance (g_d), and drain-induced barrier lowering (DIBL) start to take place. G. H. Jessen *et al.* showed that a ratio of at least 6 or larger of gate length (L_g) to gate-to-channel distance (d) should be achieved to have no strong V_{TH} reduction. In addition, a maximum g_m is achieved by having a ratio of about 5 of L_g to d, as shown in Figure 2.6 and Figure 2.7 [12].

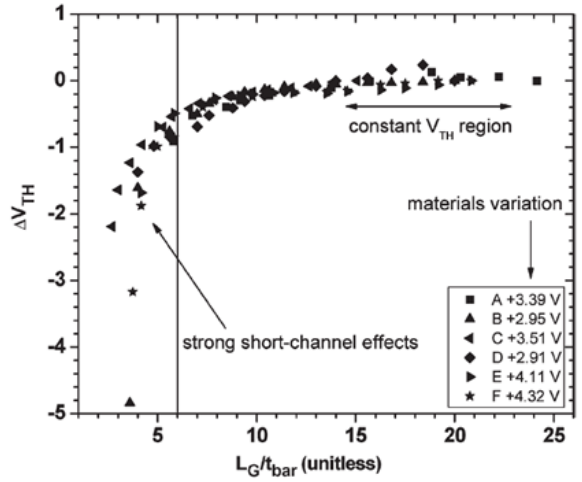

Figure 2.6. Behavior of V_{TH} with respect to the ratio of L_g to gate-to-channel distance (d). © IEEE 2007. Reprinted, with permission, from [12].

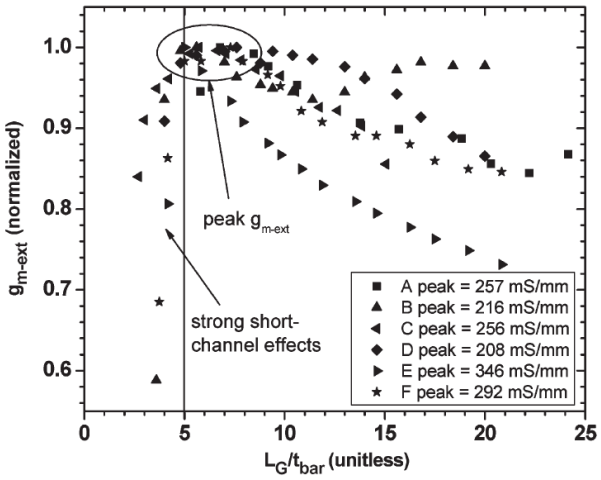

Figure 2.7. Behavior of gm with respect to the ratio of L_g to gate-to-channel distance (d). © IEEE 2007. Reprinted, with permission, from [12].

2.3 State-of-the-art technology and prospects

To the best of the author's knowledge, the current state-of-the-art high-speed depletion-mode GaN HEMT is reported in [13] with f_T/f_{max} of 454/444 GHz and an OFF-state breakdown voltage of 10 V. The devices are fabricated on a double heterojunction AlN/GaN/AlGaN epitaxial structure on SiC substrate with a 2DEG mobility and a sheet concentration of 1200 cm^2/V-s and

1.2×10^{13} cm^{-2}, respectively. Via electron beam lithography, a 20-nm L_g and 50-nm-wide gate–source and gate–drain separation are realized and inherently allow low intrinsic delay. In addition, T-shape gate is utilized to provide sufficient degree of freedom in simultaneously minimizing gate-related parasitic capacitance and gate contact resistance that benefit f_T and f_{max}, respectively, by tuning the gate foot height and gate head width (Figure 2.8). More importantly, as shown in Figure 2.9, heavily doped n-type GaN is used for source and drain regions, aka the so-called 3D-2D contacts, for minimizing R_s and R_d and thus the ON-state channel resistance (0.26 Ω–mm at V_{GS} = 2 V). Overall, the achieved Johnson figure of merit of 4.5 THz-V clearly demonstrates the promising capability of GaN HEMT in supporting 5G telecommunication technology and beyond.

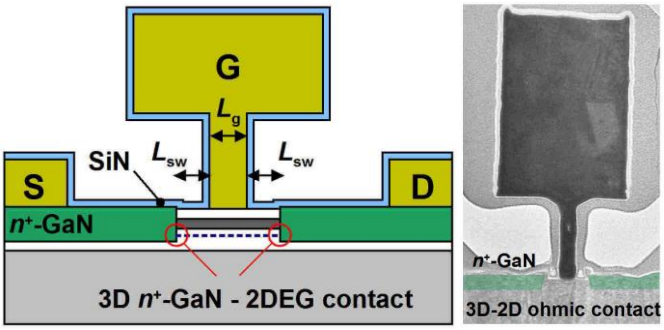

Figure 2.8. Schematic and TEM cross section images of the fabricated device. © IEEE 2013. Reprinted, with permission, from [5].

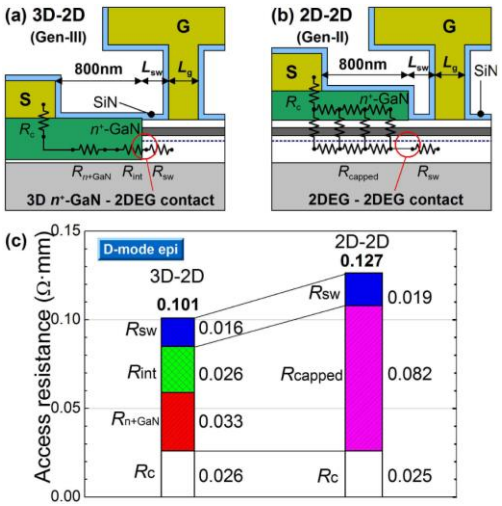

Figure 2.9. Illustration of the 3D-2D contact for minimizing parasitic resistance. © IEEE 2013. Reprinted, with permission, from [5].

CHAPTER 3 EFFECT OF RESIDUAL EPITAXIAL STRAIN ON 2-D ELECTRON GAS (2DEG) MOBILITY AND AlGaN/GaN HEMTS

AlGaN/GaN high-electron-mobility transistor (HEMT) structures are grown on 200 mm diameter Si(111) substrates by using three different buffer layer configurations: (a) thick-GaN / 3 × {$Al_xGa_{1-x}N$} / AlN, (b) thin-GaN / 3 × {$Al_xGa_{1-x}N$} / AlN, and (c) thin-GaN / AlN, so as to have crack-free and low-bow (< 50 μm) wafer. Scanning electron microscopy, energy-dispersive X-ray spectroscopy, high-resolution cross-section transmission electron microscopy, optical microscopy, atomic-force microscopy, cathodoluminescence, Raman spectroscopy, X-ray diffraction ($\omega/2\theta$ scan and symmetric/asymmetric ω scan (rocking curve scan), reciprocal space mapping) and Hall effect measurements are employed to study the structural, optical, and electrical properties of these AlGaN/GaN HEMT structures. The effects of buffer layer stacks (i.e. thickness and content) on defectivity, stress, and two-dimensional electron gas (2DEG) mobility and 2DEG concentration are reported. It is shown that 2DEG characteristics are heavily affected by the employed buffer layers between AlGaN/GaN HEMT structures and Si(111) substrates. Particularly, we report that in-plane stress in the GaN layer affects the 2DEG mobility and 2DEG carrier concentration significantly. Buffer layer engineering is shown to be essential for achieving high 2DEG mobility (> 1800 cm^2/V-s) and 2DEG carrier concentration (> 1.0×10^{13} cm^2) on Si(111) substrates.

3.1 Introduction

AlGaN/GaN high-electron-mobility transistors (HEMTs) are being investigated for high-power and high-frequency applications as III-nitride (i.e. GaN) materials have high thermal and

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chemical stability, high breakdown field (> 3 MV/cm, 10 times of that of silicon), and high electron saturation velocity (> 2.5×10^7 cm/s, 2.5 times of that of silicon) [4], [15], [16]. AlGaN/GaN HEMTs are traditionally grown on sapphire (Al_2O_3) or silicon carbide (6H-SiC) substrates that have ~16% and ~3% lattice-mismatch with GaN, respectively [17]. Recently, high cost and limited diameter-scalability of these substrates fueled the research for the GaN-on-silicon (111) approach [18]. However, the lattice mismatch of ~17% combined with the thermal-expansion-coefficient mismatch of ~54% between GaN and Si(111) necessitate employment of novel (Al)GaN buffer layers to minimize mismatch-effects (i.e. defectivity and wafer-bow) [19]. It is reported that several micrometer-thick buffer layers and various Al-content $Al_xGa_{1-x}N$ layers are needed to mitigate such detrimental effects of lattice and thermal-mismatches [20]. Nonetheless, performance of AlGaN/GaN HEMTs is governed by the two-dimensional electron gas (2DEG), which forms at the AlGaN-GaN hetero-interface, and without the need of any doping – thanks to the high conduction band offset and polarization fields between AlGaN and GaN [7]. Particularly, a high 2DEG density reduces the source/drain contact resistance [21] and increases the power output of AlGaN/GaN HEMTs [16] whereas high 2DEG mobility increases the frequency performance of AlGaN/GaN HEMTs [22]. It is therefore imperative to study the characteristics of the 2DEG and investigate how 2DEG characteristics change under various buffer layer configurations. To do so, the same AlGaN/GaN HEMT structures need to be grown on Si(111) but with various buffer layers [20]. Another important milestone in GaN-on-Si(111) technology is Si(111) wafer-scaling. Despite the early works on 100 mm substrates [23], it is critical to scale these efforts to 200 mm substrates. This, however, is bottlenecked primarily by the large GaN-Si thermal mismatch that introduces high stress leading to significant wafer-bow [24] or worse, wafer cracking [25].

In this work, we grew the same AlGaN/GaN HEMT structures on 200 mm Si(111) substrates using three different buffer layer configurations {such that all wafers are crack-free and have a small bow (< 50 μm)} and report the effects of buffer layers on the AlGaN/GaN HEMT structures. To quantify the stress and defectivity, we investigate these stacks using structural, optical and electrical characterization techniques including scanning electron microscopy (SEM), energy-dispersive X-ray spectroscopy (EDS), high-resolution cross-sectional transmission electron microscopy (HR-XTEM), optical microscopy, atomic-force microscopy (AFM), cathodoluminescence (CL), Raman spectroscopy, X-ray diffraction (XRD) {$\omega/2\theta$ scan, symmetric/asymmetric ω scan (rocking curve scan), and reciprocal space mapping (RSM)} and Hall effect measurements. Then we correlate the electrical properties of AlGaN/GaN HEMT structures with the embodied buffer layer properties and report the effects of buffer layer stress and defectivity on the 2DEG mobility and 2DEG concentration.

3.2 Investigation of AlGaN/GaN HEMT structures and the underlying buffer layer configurations

Figure 3.1 shows the AlGaN/GaN HEMT structures grown on Si(111) substrate with three different buffer configurations: (a) thick-GaN / 3 × {$Al_xGa_{1-x}N$} / AlN (Sample A), (b) thin-GaN / 3 × {$Al_xGa_{1-x}N$} / AlN (Sample B), and (c) thin-GaN / AlN (Sample C). Hitachi S-4700/S-4800 high-resolution SEM is used to measure layer thicknesses. All three configurations employ an AlN buffer layer (240-nm-thick, 175-nm-thick, and 130-nm-thick in samples A, B, and C, respectively) on top of the Si(111) substrate to prevent Ga-etch back during (Al)GaN growth [26]. On top of the AlN buffer layers, samples A and B have three step-graded $Al_xGa_{1-x}N$ buffer layers (400-nm-thick $Al_{0.33}Ga_{0.67}N$ / 290-nm-thick $Al_{0.60}Ga_{0.40}N$ / 200-nm-thick $Al_{0.82}Ga_{0.18}N$ in sample A and 240-nm-thick $Al_{0.30}Ga_{0.70}N$ / 210-nm-thick $Al_{0.58}Ga_{0.42}N$ / 190-nm-thick $Al_{0.82}Ga_{0.18}N$ in sample B)

whereas sample C has no AlGaN buffer layer. Then, 2280-nm-thick n-doped (n-) followed by 2880-nm-thick intrinsic (i-) GaN layers were grown for sample A whereas only 1200- and 950-nm-thick intrinsic GaN layers were deposited on samples B and C, respectively. Atop of all samples, the same AlGaN/GaN HEMT structure, composed of 2-nm-thick i-GaN / 17-nm-thick $Al_xGa_{1-x}N$ / 1-nm-thick AlN, was deposited. Figure 3.1 (d) shows HR-XTEM and CL of the AlGaN/GaN HEMT structure. Intrinsic GaN cap protects the $Al_xGa_{1-x}N$ barrier layer surface and minimizes the electrical contact resistance for Hall measurements [27]. To minimize layer relaxation through defect generation at the $Al_xGa_{1-x}N$-GaN hetero-interface, only a 17-nm-thick $Al_xGa_{1-x}N$ barrier layer (measured by HR-XTEM) is grown [28]. We also employed CL spectroscopy (JEOL 7000F analytical Schottky field emission SEM equipped with Gatan MonoCL3 CL Spectrometer) to probe the bandgap energy of the $Al_xGa_{1-x}N$ barrier layer for estimating the Al composition. Cathodoluminescence measurement was conducted with 5x magnification, 1.5 kV electron acceleration voltage (which yields a 29-nm penetration depth based on Kanaya-Okayama formula [29]), and 2 nA current. The measured spectrum was fitted using Gaussian distribution and the peak positions were obtained as 3.924 eV, 3.882 eV, and 3.874 eV for sample A, B, and C, respectively. Based on the peak position, we calculated the Al composition (x) of the $Al_xGa_{1-x}N$ barrier layer to be 0.25, 0.23, and 0.22 for sample A, B, and C, respectively [30]. The AlN spacer layer is inserted between the $Al_xGa_{1-x}N$ barrier and GaN to increase the conduction band offset and the 2DEG confinement in order to increase 2DEG concentration and mobility [31], [32]. Overall, samples A, B, C have the total epilayer thickness of 6.3, 2.0, and 1.2 µm, respectively (Figure 3.1).

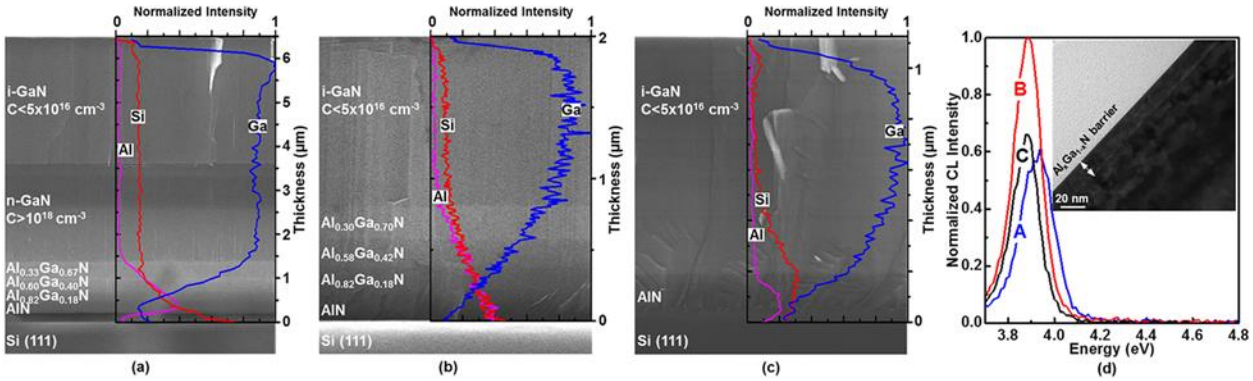

Figure 3.1. SEM cross section, EDS, HR-XTEM, and CL investigations of the AlGaN/GaN HEMT structures grown on Si(111) substrate with three different buffer configurations. (a) Thick-GaN / 3 × {$Al_xGa_{1-x}N$} / AlN (Sample A), (b) Thin-GaN / 3 × {$Al_xGa_{1-x}N$} / AlN (Sample B), and (c) Thin-GaN / AlN (Sample C). Atop of all samples (A, B, C), the same AlGaN/GaN HEMT structure, composed of 2-nm-thick i-GaN / 17-nm-thick $Al_xGa_{1-x}N$ / 1-nm-thick AlN, is deposited as shown in (d). Based on the CL spectrum peak position of the $Al_xGa_{1-x}N$ barrier layer, Al composition can be estimated as 0.25, 0.23, and 0.22 for sample A, B, and C, respectively [14].

The critical elemental compositions (i.e. Al, Ga, Si) across these samples (i.e. A, B, C) are investigated by Oxford Instrument ISIS EDS X-ray microanalysis system with a spatial resolution of ~ 1 μm and plotted in Figure 3.1. In samples A and B, from GaN layer towards the Si(111) substrate, the Ga signal decreases as the Al signal increases, as we have step-graded $Al_xGa_{1-x}N$ layers. In sample C a rather rounded Al signal peak is observed as it has no step-graded $Al_xGa_{1-x}N$ layers. The Si signal increases in all samples towards the substrate showing the Si diffusion.

3.3 Surface investigation of the AlGaN/GaN HEMT structure via optical microscopy, atomic force microscopy, and cathodoluminescence

Figure 3.2 shows the surface studies of all samples (A, B, C) by optical microscopy (Figure 3.2 (a), (b), (c)), atomic force microscopy (Figure 3.2 (d), (e), (f)) and CL (Figure 3.2 (g), (h), (i)). No surface cracks are observed in any samples, indicating high film quality [25]. Atomic force microscopy (Asylum Cypher S AFM with tapping mode) is used to study the surface roughness and contour of the AlGaN/GaN HEMT structures. Figure 3.2 (d), (e), (f) show 5 μm × 5 μm AFM

scans. It is important to note that the average root-mean-square (RMS) roughnesses are similar across samples (5.5 ± 2.8, 5.2 ± 1.4, and 5.1 ± 1.3 Å, for A, B, and C, respectively), wherein sample A has the largest surface roughness. In order to quantify surface-terminated defects (i.e. dislocations with threading component), we counted the "dark spots" on the AFM images (Figure 3.2 (d), (e), (f)) [33] which averaged as $1.8 \pm 0.3 \times 10^9$, $2.2 \pm 0.8 \times 10^9$, and $2.6 \pm 0.8 \times 10^9$ cm^{-2} (Table 3.1) for samples A, B, and C, respectively, showing thickest sample (A) having the lowest density of threading type dislocations, in agreement with other works [34], [35]. Based on their different sizes these dark spots can be classified as pure-edge type (small), pure-screw type (large) and mixed-type (middle) threading dislocations.

Cathodoluminescence is also a useful tool in highlighting the surface defects as defects are centers of non-radiative recombination and appear dark in a panchromatic view [36]. We again employed the same CL spectroscopy system to study these samples. A panchromatic CL image using a 2.0 kV electron acceleration voltage (that gives a penetration depth of 47 nm [29]) reveals the defect distribution as shown in Figure 3.2 (g), (h), (i). The average CL defectivity for samples A, B, and C are measured as $1.0 \pm 0.3 \times 10^9$, $2.0 \pm 0.3 \times 10^9$, and $1.8 \pm 0.3 \times 10^9$ cm^{-2} (Table 3.1), respectively. This suggests, similar to our AFM results, that the thickest sample A has the least defectivity. With respect to AFM analysis, CL underestimates the defectivity because defects have capture radius, suggesting that multiple defects are located within one CL dark capture radius.

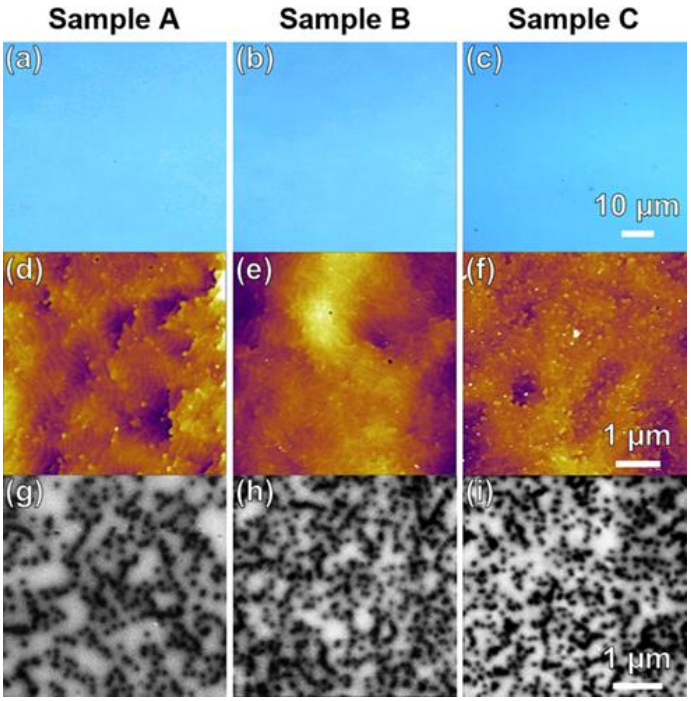

Figure 3.2 Optical microscopy, AFM and CL images of samples A, B and C. Optical microscopy (a, b, c) reveals no surface cracks. AFM (d, e, f) reveals the average root-mean-square (RMS) roughness of 5.5 ± 2.8, 5.2 ± 1.4, and 5.1 ± 1.3 Å for sample A, B, and C, respectively, suggesting a similar surface profile. Cathodoluminescence (g, h, i) reveals defectivity of sample A, B, and C as $1.0 \pm 0.3 \times 10^9$, $2.0 \pm 0.3 \times 10^9$, $1.8 \pm 0.3 \times 10^9$ cm^{-2}, respectively. AFM and CL studies agree that sample A (the thickest sample) has the lowest threading dislocation defect density whereas sample C (the thinnest sample) has the highest one (Table 3.1) [14].

Table 3.1. Structural (surface roughness, defectivity, stress) and electrical (contact resistance, 2DEG concentration, 2DEG mobility) properties of samples A, B, and C.

Sample (Epi thickness)	**AFM surface roughness (Å)**	**Defectivity (10^9 cm^{-2})**				**GaN stress (GPa)**		**Electrical property**					
		AFM	**CL**	**XRD**		**XRD**	**Raman**	***R*$_s$ (Ω/□)**		**2DEG *N*$_s$ (10^{13} cm^{-2})**		**2DEG μ_n (cm^2/V-s)**	
				***D*$_{screw}$**	***D*$_{edge}$**	**Tensile**	**Compressive**	**RT**	**77 K**	**RT**	**77 K**	**RT**	**77 K**
A (6.3 µm)	5.5 ± 2.8	1.8 ± 0.3	1.0 ± 0.3	0.40	1.02	1.059	0.256	431.8 ±109.8	110.8 ± 28.1	1.20 ± 0.01	1.30 ± 0.10	1295 ± 247	4867 ± 996
B (2.0 µm)	5.2 ± 1.4	2.2 ± 0.8	2.0 ± 0.3	0.58	1.47	0.154	0.488	385.8 ± 28.1	66.5 ± 5.0	0.89 ± 0.01	1.00 ± 0.01	1802 ± 102	9175 ± 698
C (1.1 µm)	5.1 ± 1.3	2.6 ± 0.8	1.8 ± 0.3	0.39	1.02	1.548	0.047	445.5 ± 75.3	96.0 ± 23.0	0.92 ± 0.05	1.00 ± 0.10	1593 ± 268	6930 ± 1541

3.4 Layer stress analysis through Raman measurements, X-ray diffraction and reciprocal space mapping

We studied the GaN stress via Horiba Raman Confocal Imaging Microscope using 633-nm laser line (with a grating of 1800 lines/mm, yielding a resolution of 1.19 cm^{-1}). Under Z(XX)-Z configuration, E_2^H and A1(LO) Raman peaks are measured, and the shifts in these Raman peaks from the stress-free values of 567.5 cm^{-1} (E_2^H) at 300 K are recorded. Based on the shift direction and the shift amount ($\Delta\omega$) of E_2^H, we determined the stress type as compressive and calculated the stress amount (σ_xx) through [23]

$$\sigma_{xx} = \frac{\Delta\omega}{4.3}\,\mathrm{cm}\cdot\mathrm{GPa} \tag{3.1}$$

and tabulated them in Table 3.1. The Raman spectra of sample A, B, and C are also plotted in Figure 3.3. Our Raman spectroscopy investigation suggests that sample B is under the largest compressive stress (0.488 GPa) whereas sample C is under the smallest compressive stress (0.047 GPa) and sample A has the medium value (0.256 GPa). These results are similar to other Raman works on AlGaN/GaN HEMT structures on Si(111) [23].

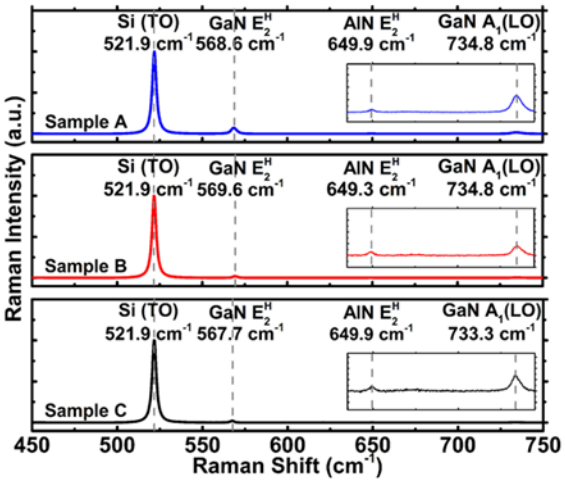

Figure 3.3 Raman spectroscopy of all samples A, B, and C [14].

We further quantify the (Al)GaN layers' composition, strain, and defect density via XRD [37], [38]. Here we employ PANalytical/Philips X'pert MRD system with 0.154-nm-wavelength radiation to study all samples. Omega/2Theta (ω/2θ) scan is used to probe the symmetrical lattice plane (0002) to determine the Al compositions of the $Al_xGa_{1-x}N$ buffer layers according to:

$$x_{Al} = \left(c_{Al_xGa_{1-x}N} - c_{GaN}\right) / \left(c_{AlN} - c_{GaN}\right), \tag{3.2}$$

where c represents the lattice constant along the c axis calculated via Vegard's law [39]. Figure 3.4 shows the ω/2θ scans of samples A, B, and C. The narrowest FWHM of sample B indicates the highest crystalline order amongst the samples, whereas sample A has the lowest crystalline order indicated by its widest FWHM. However, one should be aware that the Al composition results obtained from XRD ω/2θ scan can be inaccurate since both the epilayer strain and alloy composition will significantly affect the peak position of the ω/2θ scan; to estimate the Al composition more precisely, XRD reciprocal space mapping is necessary.

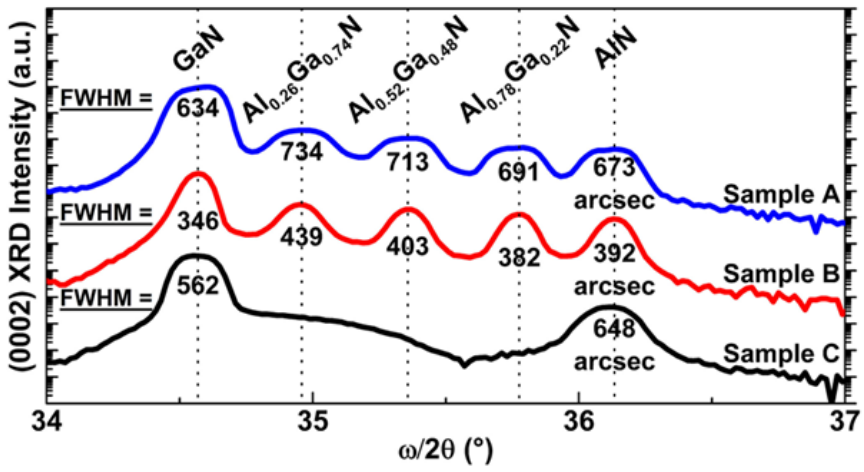

Figure 3.4 Symmetric XRD ω/2θ scans of samples A, B, and C are used to determine the Al-content and crystalline quality. Results show sample B having the narrowest FWHM values, suggesting the best crystallography quality among all samples [14].

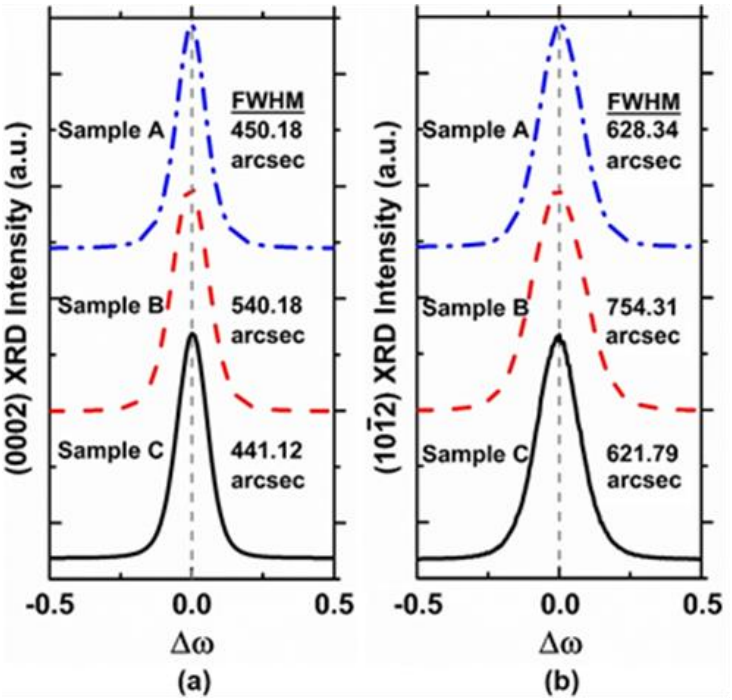

Figure 3.5 (a) Symmetric and (b) asymmetric ω (rocking curve) scans of (0002) and (101$\bar{2}$) lattice planes are shown. Symmetric ω scan on (0002) plane is used for investigating the screw-type threading dislocation density and asymmetric ω scan on (101$\bar{2}$) plane is used for edge-type threading dislocation density investigation (Table 3.1) [14].

In addition, we conducted (0002) (symmetric) and $(10\bar{1}2)$ (asymmetric) ω scans to estimate the densities of screw-type (Burgers vector length: 0.5185 nm (b_{screw})) and edge-type (Burgers vector length: 0.3189 nm (b_{edge})) threading dislocations, respectively (Figure 3.5) [37], [40], [41]. Based on the FWHM of (0002) (symmetric) and $(10\bar{1}2)$ (asymmetric) ω scans (i.e. β_((0002)) and β_($(10\bar{1}2)$)), screw- and edge-type threading dislocation densities (D_{screw} and D_{edge}) are estimated via [37], [40], [41]:

$$D_{screw} = \frac{\beta^2_{(0002)}}{4.35 b^2_{screw}} \tag{3.3}$$

$$D_{\text{edge}} = \frac{\beta^2_{(10\bar{1}2)} - \beta^2_{(0002)}}{4.35 b^2_{\text{edge}}} \tag{3.4}$$

and tabulated in Table 3.1. Our XRD analysis suggests that sample A and C have similar amount of pure-edge- and screw-type threading dislocation densities.

X-ray diffraction reciprocal space mappings of (0002) and $(10\bar{1}5)$ planes (Figure 3.6) are performed to quantify the (Al)GaN layers' strain and stress; in addition, the Al composition can be more precisely quantified compared to the $\omega/2\theta$ scan. Lattice constants a and c of each layer (GaN, $Al_xGa_{1-x}N$, AlN) are obtained from Figure 3.6 via the equation:

$$\left(\frac{1}{d_{\text{hkl}}}\right)^2 = \frac{4}{3}\left(\frac{h^2 + hk + k^2}{a^2}\right) + \frac{l^2}{c^2}, \tag{3.5}$$

where d_{hkl} represents the interplanar spacing of the probed lattice plane (hkl) [42]. Employing the Poisson-Vegard's law [42] while including the lattice constant bowing parameter [43], the Al composition (x), the free-standing lattice constants (a_0(x) and c_0(x)), and the in-plane (ε_{xx}) and out-of-plane strain (ε_{zz}) of each layer are calculated via:

$$\begin{cases} \dfrac{c_m(x) - c_0(x)}{c_0(x)} = -\dfrac{2\nu(x)}{1-\nu(x)} \times \dfrac{a_m(x) - a_0(x)}{a_0(x)} \\ c_0(x) = x c_{\text{AlN}} + (1-x) c_{\text{GaN}} + \delta_c \cdot x \cdot (1-x) \\ a_0(x) = x a_{\text{AlN}} + (1-x) a_{\text{GaN}} + \delta_a \cdot x \cdot (1-x) \\ \nu_0(x) = x \nu_{\text{AlN}} + (1-x) \nu_{\text{GaN}}, \end{cases} \tag{3.6}$$

where

$$\varepsilon_{xx} = \left[a_m(x) - a_0(x)\right] / a_0(x), \tag{3.7}$$

$$\varepsilon_{zz} = \left[c_m(x) - c_0(x)\right] / c_0(x) \tag{3.8}$$

$a_m(x)$ and $c_m(x)$ are the measured lattice constants; a_{AlN} = 3.112 Å, c_{AlN} = 4.982 Å, a_{GaN} = 3.186 Å, and c_{AlN} = 5.186 Å, representing free-standing lattice constants. The Poisson ratio v_{AlN} and v_{GaN} are 0.203 and 0.183, respectively [42]. δ_c and δ_a represent the deviation (bowing) parameter and were fit to be -0.036 and 0.018 Å, respectively [43]. The in-plane stress (σ_{xx}) is also calculated according to:

$$\sigma_{xx} = \left[\left(C_{11} + C_{12} \right) - 2C_{13}^{\ 2} / C_{33} \right] \times \varepsilon_{xx}, \tag{3.9}$$

where C_{ij} are the elastic constants of GaN (C_{11} = 390 GPa, C_{12} = 145 GPa, C_{13} = 106 GPa, and C_{33} = 398 GPa) [44]. The resulting in-plane stress values of GaN layers are tabulated in Table 3.2. The in-plane strains of each (Al)GaN layer of the three samples are also plotted in Figure 3.7. For sample A and B, from the AlN layer toward the $Al_xGa_{1-x}N$ layers the in-plane strain first decreases from positive (tensile), crosses the zero line (strain-free), and then becomes negative (compressive). Finally, the in-plane strain returns to positive (tensile) due to the growing of the GaN layer. This discovered trend agrees with a previous work [45] where the in-plane strain in a GaN/Al_xGa_{1-x}N/AlN system initially decreases along with the increase of the structure thickness and then crosses the zero line; as the GaN gets thicker the slope gets less steep, suggesting that an in-plane strain with a tensile component launches and becomes more dominant as the GaN thickness increases.

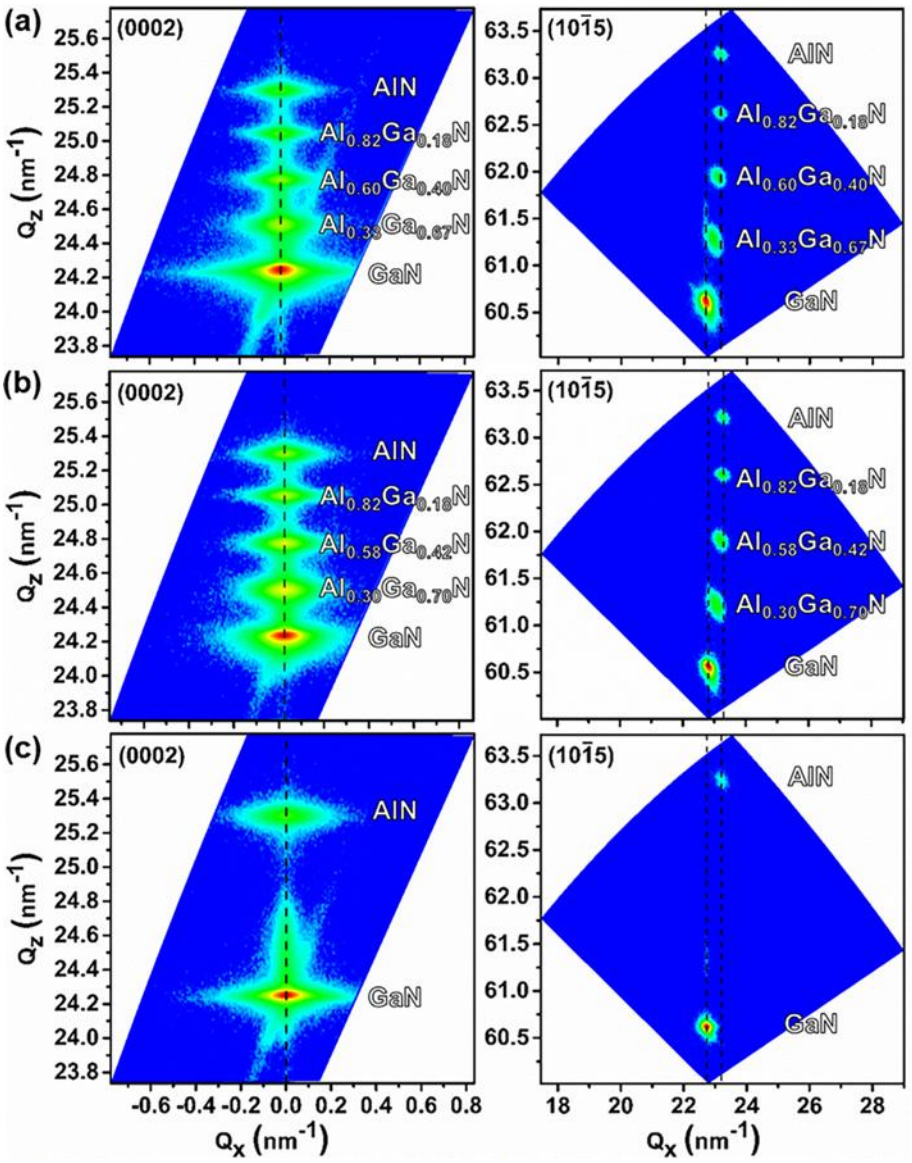

Figure 3.6. XRD reciprocal space mapping results reveal that the GaN layers of all samples (A, B, C) are under tensile strain along the c-plane and are under compressive strain normal to the c-plane. Sample B is observed to have the lowest GaN in-plane stress (Table 3.1) [14].

Our XRD RSM results suggest that the GaN layers of all three samples have tensile stress with sample B having the lowest stress (~ 0.154 GPa), sample C having the highest one (~ 1.548 GPa), and sample A having a medium value (~ 1.059 GPa). This indicates that the step-graded AlxGa1-xN layers used in samples A and B reduce the in-plane (tensile) stress of the GaN layer. Moreover, GaN in sample A is shown to have a higher in-plane tensile stress than GaN in sample

B. We attribute this to sample A having a thicker GaN layer (a thicker i-GaN layer and an additional n-GaN layer) than sample B. Moreover, it has been reported that smaller-sized dopants, such as Si, in GaN films will form impurity atmospheres that limit the dislocation movement while growing, which further limits the dislocation reduction and the relief of the GaN tensile stress [46]. At this stage, we fairly believe that the carbon dopant in the n-doped GaN in sample A has an equivalent effect on enlarging the GaN film tensile stress. This indicates the importance of optimal buffer layer configuration in terms of thicknesses and Al-content.

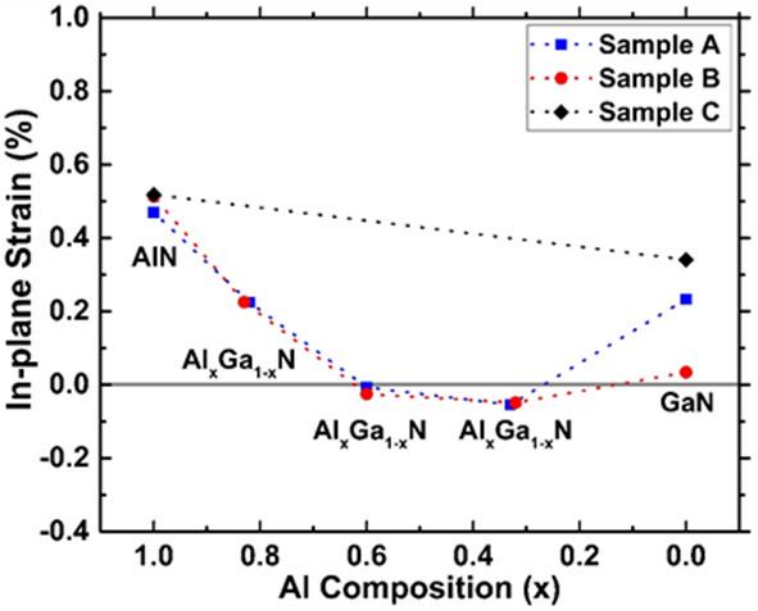

Figure 3.7. In-plane strain of GaN, AlxGa1-xN, and AlN obtained from XRD reciprocal space mapping are demonstrated. For sample A and B, from the AlN layer to the $Al_xGa_{1-x}N$ layer the in-plane strain first decreases from positive (tensile), crosses the zero line (strain-free), and then becomes negative (compressive). Finally, the in-plane strain returns to positive (tensile) due to the growth of the GaN layer. Sample A has a thicker GaN layer than sample B, which results in the higher in-plane tensile strain of the GaN layer. Without any $Al_xGa_{1-x}N$ buffer layer, the GaN in-plane tensile strain of sample C is investigated to be the largest one [47].

Table 3.2. XRD reciprocal space mapping calculations are tabulated. The free-standing lattice constants (a_0/c_0) and elastic constants of $Al_xGa_{1-x}N$ are calculated using Poisson-Vegard's law with bowing parameter correction [14].

Sample (Epi thickness)	Layers	Measured lattice constant (a/c) (Å)	Free-standing lattice constant (a_0/c_0) (Å)	In-plane strain/stress (%)/(GPa)	Out-of-plane strain (%)
A (6.315 μm)	GaN	3.1936/5.1827	3.1860/5.1860	+0.2331/+1.0586	-0.0629
	$Al_{0.33}Ga_{0.67}N$	3.1558/5.1275	3.1574/5.1262	-0.0540/-0.2364	+0.0253
	$Al_{0.60}Ga_{0.40}N$	3.1371/5.0730	3.1375/5.0728	-0.0067/-0.0283	+0.0032
	$Al_{0.82}Ga_{0.18}N$	3.1295/5.0176	3.1224/5.0232	+0.2246/+0.9185	-0.1119
	AlN	3.1266/4.9678	3.1120/4.9820	+0.4699/+1.8659	-0.2849
B (2.007 μm)	GaN	3.1873/5.1855	3.1860/5.1860	+0.0340/+0.1544	-0.0088
	$Al_{0.30}Ga_{0.70}N$	3.1567/5.1295	3.1583/5.1283	-0.0487/-0.2140	+0.0228
	$Al_{0.58}Ga_{0.42}N$	3.1365/5.0726	3.1372/5.0720	-0.0250/-0.1059	+0.0121
	$Al_{0.82}Ga_{0.18}N$	3.1290/5.0161	3.1220/5.0217	+0.2254/+0.9218	-0.1124
	AlN	3.1279/4.9674	3.1120/4.9820	+0.5134/+2.0387	-0.2933
C (1.125 μm)	GaN	3.1968/5.1815	3.1860/5.1860	+0.3408/+1.5477	-0.0872
	AlN	3.1283/4.9670	3.1120/4.9820	+0.5181/+2.0573	-0.3004

3.5 Investigation of the two-dimensional electron gas characteristics via Hall effect measurement

Hall effect measurements under Van der Pauw configuration are carried out at room (300 K) and low (77 K) temperatures. The metal contacts are formed via e-beam evaporation of 200-nm-thick Ti / 200-nm-thick Ni metal stack and annealed at 750 °C under N_2 for 45 seconds. Samples are then diced into 5 mm × 5 mm squares and measured under Van der Pauw configuration.

Carrier concentration (N_s), sheet resistance (R_s), and mobility (μ_n) of samples A, B, and C are tabulated in Table 3.1. The 2DEG concentration is the highest in sample A, whereas 2DEG mobility is highest in sample B. It was earlier reported that carrier concentration and mobility of a 2DEG system are strongly related [48]. At high 2DEG carrier concentration ($> \sim 2 \times 10^{12}$ cm^{-2}), the 2DEG mobility has a negative dependence on increasing carrier concentration due to the surface roughness scattering, in agreement with our work. At low temperature (77 K), the 2DEG

mobility increases and the sheet resistance decreases in all samples due to the reduced phonon scattering at low (77 K) temperature. Furthermore, 2DEG concentrations in all our samples are higher at 77 K than at 300 K, in line with other works [49].

3.6 Discussion

Our defectivity measurements via AFM and CL reveal that threading dislocation density reduces with increasing total buffer thickness. We further show that step-graded AlGaN buffer layers and thicker GaN buffer layers alone are beneficial in doing so. This is attributed to the interaction of edge- and mixed-type threading dislocations in the forms of fusion (i.e. two threading dislocation lines merging into one) and annihilation (two threading dislocation lines (having opposite Burgers vectors) annihilating one another) [26]. As the (Al)GaN film is further deposited, the possibility of such interactions increases, lowering the threading dislocation density. In particular, the inaccuracy of CL and XRD defectivity measurements is discussed here. As mentioned, CL measurement tends to underestimate the defectivity because these defects act as non-radiative recombination centers that possess capture radius; compared to AFM defectivity, the lower defectivity of CL suggests that multiple defects are located within one CL dark capture radius. On the other hand, the estimated XRD defectivity here provides information about the densities of the pure-screw- and pure-edge-type threading dislocations; mixed-type threading dislocation, which typically occupies a large portion of the total defectivity, is not evaluated. In addition, although we conduct asymmetric rocking curve scan on the commonly used $(10\bar{1}2)$ plane to estimate the pure-edge-type threading dislocations, the measured XRD rocking curve FWHM is not solely affected by threading dislocations; other factors such as instrumental broadening, microstrain, and wafer curvature also play roles in changing the FWHM [37]. We suggest taking the AFM defectivity as the total defectivity as it is the most direct and sensitive one, which

concludes that sample C should possess a large amount of mixed-type threading dislocations that leads to its largest total defectivity.

X-ray diffraction RSM is used to investigate strain distribution in buffer layers (Figure 3.6 and Figure 3.7) providing in-/out-of-plane strain information of GaN, $Al_xGa_{1-x}N$, and AlN layers as shown in Table 3.2. In samples A, B and C, the AlN in-plane tensile strains are found to be 0.47%, 0.51%, and 0.52%, respectively. We observe a gradual reduction of in-/out-of-plane tensile strain in the step-graded 3 × $\{Al_xGa_{1-x}N\}$ buffer layers from Si(111) towards the AlGaN/GaN HEMT structure (Table 3.2 and Figure 3.7). This leads to a lower tensile GaN in-plane strain in samples A (0.23%) and B (0.03%) than that in sample C (0.34%), showing the importance of step-graded $Al_xGa_{1-x}N$ buffer layers. Between sample A and B, GaN in-plane tensile strain in sample B is lower than that in sample A, leading to a narrower XRD FWHM (Figure 3.6), although Raman spectroscopy reveals a blue shift of GaN E_2^H Raman peak in all samples, which corresponds to an in-plane compressive stress (< 0.5 GPa), in line with other Raman works [23]. The discrepancy between the stress results from XRD RSM and Raman spectroscopy has been found in previous works [50], [51], which is suggested to be attributed to the fact that the stress measured by XRD RSM is an average value throughout the whole structure where the effects brought by local/random lattice distortion and/or any other imperfections are averaged out. On the other hand, the stress investigated by Raman spectroscopy is only from the spot-size area; therefore, the value is statistically insufficient and less accurate to represent the strain in the whole GaN layer. In addition, it is reported that the discrepancy will also occur when the material is doped and/or with impurities [50]. Furthermore, stress investigation using Raman spectroscopy requires a phonon-shift estimation model, which might need to be modified for short period hetero-interfaces such as

AlGaN/GaN HEMTs. Thus, we believe XRD RSM to be a more reliable means of probing the stress in thick hetero-interfaced layers than Raman studies.

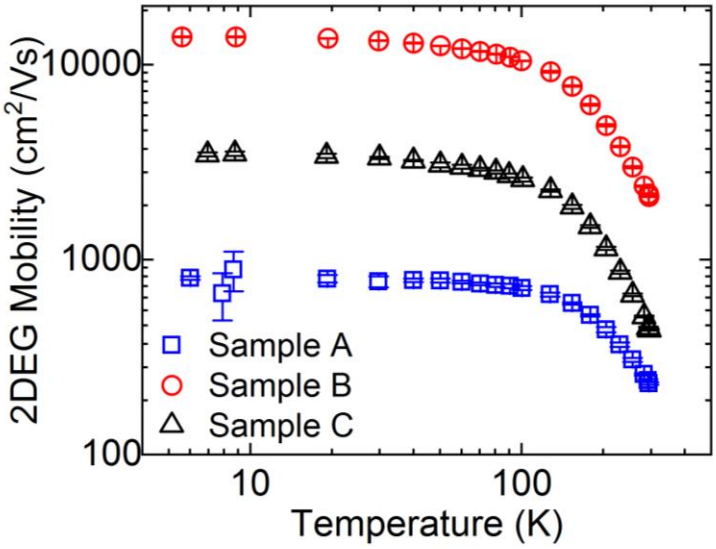

Figure 3.8. Temperature-dependent Hall measurements [Communication with Air Force Research Laboratory].

Hall effect measurements under Van der Pauw configuration are carried out to determine 2DEG concentration, sheet resistance, and 2DEG mobility (Table 3.2), and temperature-dependent Hall measurements are also performed as shown in Figure 3.8. Sheet resistance is inversely related to the 2DEG mobility; however, the relatively large variation of the sheet resistance of sample A and C should be attributed to the surface variation across the samples as the surface morphology is significantly affected by defects. As the defect density and type are varied, it is typical to have a varying surface morphology, and such variation in surface morphology greatly affects the contacts as defects are charged and some defects have threading component (during annealing metal is diffused further). The 2DEG concentration is the highest in sample A and the lowest in sample B whereas the 2DEG mobility is the highest in sample B and the lowest in sample A, showing a trade-off between 2DEG concentration and 2DEG mobility [48]. Considering that sample A has the lowest threading dislocations, but sample B has the lowest in-plane strain, our

work suggests that 2DEG mobility is not only affected by threading dislocations but also by GaN in-plane strain. As 2DEG concentration is affected by the spontaneous (P_{SP}) and piezoelectric (P_{PE}) polarizations in the $Al_xGa_{1-x}N$ barrier layer and the underlying GaN layer (where the piezoelectric polarization is determined by strain [7]), a fixed polarization charge density (C/m^2) is induced at the AlGaN/GaN hetero-interface given by:

$$\begin{aligned}\sigma\left(P_{SP}+P_{PE}\right) &= P(\mathrm{GaN})-P(\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N}) \\ &= \left\{P_{PE}\left(\mathrm{GaN}\right)-P_{PE}\left(\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N}\right)\right\} \\ &+ \left\{P_{SP}\left(\mathrm{GaN}\right)-P_{SP}\left(\mathrm{Al}_x\mathrm{Ga}_{1-x}\mathrm{N}\right)\right\},\end{aligned} \tag{3.10}$$

where P_{SP} does not change with strain whereas P_{PE} follows:

$$P_{PE} = 2\frac{a-a_0}{a_0}\left(e_{31}-e_{33}\frac{C_{13}}{C_{33}}\right), \tag{3.11}$$

where (C_{13}, C_{33}) are elastic constants and (e_{31}, e_{33}) are piezoelectric coefficients. For P_{PE} (GaN), a_0 = 3.186 Å, e_{31} = – 0.49 C/m^2, e_{33} = 0.73 C/m^2, C_{13} = 103 GPa, and C_{33} = 405 GPa; for $P_{PE}(Al_xGa_{1-x}N$, x = 0.25, 0.23, and 0.22 in sample A, B, and C, respectively), $a_0 \cong$ 3.165 Å, $e_{31} \cong$ – 0.52 C/m^2, $e_{33} \cong$ 0.92 C/m^2, $C_{13} \cong$ 104.25 GPa, and $C_{33} \cong$ 397 GPa [7]. Since the $Al_xGa_{1-x}N$ barrier layer is thin (~ 17 nm), we fairly assume that it is fully strained with no relaxation, which allows us to further assume that the lattice constant a of the $Al_xGa_{1-x}N$ barrier layer should be the same as that of the GaN layer. We then obtain P_{PE} (GaN) – P_{PE} ($Al_xGa_{1-x}N$) $\cong 0.057a - 0.172$, suggesting that as lattice constant a becomes larger (meaning that both the $Al_xGa_{1-x}N$ barrier and GaN layers simultaneously stretch further under more tensile strain), {P_{PE} (GaN) – P_{PE} ($Al_xGa_{1-x}N$)} value and hence the polarization charge density (σ) increase. The increase in the polarization charge density results in an increase in 2DEG concentration, in good agreement with our observations. With an increase of the piezoelectric polarization, the ground state wave function in the quantum well actually shifts towards the side of the interface, meaning that a stronger

polarization can attract the electrons to populate closer to the interface. The high 2DEG mobility of sample B is correlated to its GaN in-plane tensile strain that is distinctively lower than the other two samples. The low GaN in-plane tensile strain of sample B leads to a low piezoelectric polarization, hence lower interface roughness scattering. On the other hand, sample A and C have larger GaN in-plane tensile strains that lead to severer interface roughness scattering. According to the AFM RMS surface roughness result (5.5 Å, 5.2 Å, and 5.1 Å for sample A, B, and C respectively), sample A should have the highest interface roughness whereas sample B and C have lower ones. For sample B, due to the low piezoelectric polarization and the low interface roughness, the scattering is weaker, allowing a high 2DEG mobility. For sample A, the highest interface roughness and the second-high piezoelectric polarization make its 2DEG mobility lower than sample B and C. For sample C, although it has the lowest interface roughness, the strongest piezoelectric polarization makes its 2DEG mobility lower than sample B.

3.7 Conclusion

Scanning electron microscopy, energy-dispersive X-ray spectroscopy, high resolution-cross section transmission electron microscopy, optical microscopy, atomic-force microscopy, cathodoluminescence, Raman spectroscopy, X-ray diffraction ($\omega/2\theta$ scan, symmetric/asymmetric ω scan (rocking curve scan), and reciprocal space mapping), and Hall effect measurements are utilized to investigate AlGaN/GaN HEMT structures on Si(111) with different buffer layer configurations. We show that thicker buffer layers are beneficial for reducing the threading dislocation density, and stacked AlxGa1-xN buffer layers are critical for reducing the layer stress. Furthermore, our work suggests that the type and the magnitude of in-plane strain of the GaN layer, not the threading dislocation density, dominate the 2DEG mobility. Overall, we demonstrate the

importance of optimal buffer layer configurations for 2DEG characteristics, which might allow high-frequency AlGaN/GaN HEMT designs on Si(111) substrates.

SAMPLE PREPARATION AND CLEANING

The AlGaN/GaN heterostructures used for this investigation are cut from three different 200-mm-diameter wafers (A, B, and C) with Si(111) substrate. The epitaxy layer configurations are shown in Figure 3.1. Samples (8 pieces of sample A from the wafer A, 18 pieces of sample B from the wafer B, and 6 pieces of sample C from the wafer C) populate on the wafer approximately ~15 cm away from the center. Sample cleaning is carried out as follows: Samples are soaked in (1) hot trichloroethylene (TCE), (2) hot acetone, (3) hot methanol followed by (4) DI rinse and (5) N_2 blow dry. For steps (1-3), an ultrasonic bath cleaning is added. All steps are carried out for ~10 minutes.

METALLIZATION, ANNEALING, AND DICING OF AlGaN/GaN HEMT STRUCTURES FOR HALL MEASUREMENTS

After sample cleaning, 200 nm titanium (Ti) and then 200 nm nickel (Ni) metal contacts were deposited through a square-shaped patterned hard mask on the Hall mobility measurement samples. The metal deposition rates were kept between 1.5 and 2.0 Å/s. Rapid thermal annealing was carried out at 750 °C for 45 s under N_2 for ohmic contact formation. Then, photoresist (PR) (AZ 5214) was spun on the samples then soft-baked at 95 °C for ~10 min in order to prevent scratching or damaging the sample surface during dicing. Finally, nickel-bond dicing blade (0.051 mm thick, 3-6 micron diamond grain size) mounted on K&S 708 dicing saw is used for dicing samples into small square dies with metal contacts in the four corners. Samples were re-cleaned before measurements. Hall measurement was performed three times for each piece of sample.

Finally, we calculate the overall averages and standard deviations of the measured data from these three kinds of samples.

CHAPTER 4 OHMIC CONTACT OPTIMIZATION OF AlGaN/GaN HEMTS

4.1 Introduction

AlGaN/GaN high-electron-mobility transistors have shown promising capabilities in enabling high-power/high-frequency operations and applications. High-frequency performance of an individual device is commonly measured by its cutoff frequency (f_T). This quantity represents the frequency at which the magnification of short-circuit current gain becomes unity. The current state of the art of the f_T is 454 GHz with a 10 V breakdown voltage [5]. The cutoff frequency is subject to various delay components, mainly including the intrinsic and the parasitic charging delays, as shown in the following equation [9]

$$f_T = \frac{1}{2\pi}\left\{\frac{\left(C_{gs}+C_{gd}\right)}{g_m} + C_{gd}\cdot\left(R_s+R_d\right)\cdot\left[1+\left(1+\frac{C_{gs}}{C_{gd}}\right)\frac{g_d}{g_m}\right]\right\}^{-1}. \quad (4.1)$$

The term $(C_{gs} + C_{gs})/g_m$ represents the intrinsic delay time, which has an equivalent form of $(L_g + \Delta L_g)/v_{avg}$, where L_g is the physical gate length, ΔL_g is the excess gate length due to drain depletion and gate fringing field, and v_{avg} is the average carrier (electrons or holes) velocity. Intuitively this quantity can be interpreted as how much time the carriers take to travel through the channel under the gate region. An increase of the average carrier velocity or a shorter gate length can both reduce the intrinsic delay time. A faster average carrier velocity comes from a faster carrier mobility which is decided by the material property. However, device scaling raises issues of parasitic charging delay expressed by the other two terms in the equation. As reported in [10], the f_T of an AlGaN/GaN HEMT starts to deviate from the ideal value that is solely decided by the intrinsic delay as the gate length is downscaled below 100 nm.

The parasitic delay term $C_{gd} \cdot (R_s + R_d)$ represents the charging delay due to the source (S) and drain (D) resistance. Researches are actively in progress to minimize these two resistances by optimizing the contact metal material stack [11], and our current investigation result is reported here. According to [11], [52], [53], [54], Ti/Al/Ni/Au is one typical metal stack configuration for achieving low resistance S/D metal contact on n-type (Al)GaN layers. Through rapid thermal annealing (RTA) at high temperature, intermixing of the metal layers and the (Al)GaN layer takes place. At high temperature (typically above 800 °C), Ti reacts with N atoms that out-diffuse from the (Al)GaN layer. Not only is the formed TiN a highly conductive compound, the nitrogen vacancy left behind makes the (Al)GaN surface become highly n-type doped, largely thinning the Schottky barrier which promotes the carrier tunneling process. In addition, Ti also reacts with Al above and forms Al_3Ti which is also highly conductive. A Ti/Al ratio of 6 has been reported for a minimized contact resistance [11]. For preventing metal oxidation and promoting the contact probing quality during measurements, gold (Au) is frequently used as the outer layer. However, Au reacts with Al and forms $AuAl_2$ that not only is a highly resistive alloy but also increases metal surface roughness due to cavities created by the reduction in volume. A rough S/D metal surface can cause issues for processing and introduce additional parasitic capacitance that compromises the high-frequency performance. In order to avoid such drawback, Ni is inserted between Au and Al as a blocking layer. However, Au and Al can still react with each other given a long annealing time at a high temperature. A three-step RTA process has been proposed to alleviate such issue [55], [56]. By adding an additional annealing step at a lower temperature and longer time, the time for the high-temperature step can be shortened and the level of Al/Au reaction can therefore be reduced.

4.2 Fabrication and rapid thermal annealing experiments

For further investigating the high-temperature effect on the contact resistance using the conventional (two-step) and three-step RTA processes, several samples for transmission line measurement (TLM) are made in this work, as shown in Figure 4.1. The fabrication processes performed on an AlGaN/GaN-HEMT-on-Si(111) sample include surface treatment (HCl, NH_4OH, and $(NH_4)_2S$), ALD Al_2O_3 pre-passivation (100 cycles), ICPRIE mesa isolation, ohmic contact region opening, hot HCl surface treatment, electron beam evaporation (Ti (20 nm) / Al (120 nm) / Ni (55 nm) / Au (45 nm)), and finally rapid thermal annealing. Each metal pad is in a size of 80 × 180 μm^2 and spaced as 7, 8, 9, 10, 15, 20, 60, 80, 100, and 120 μm.

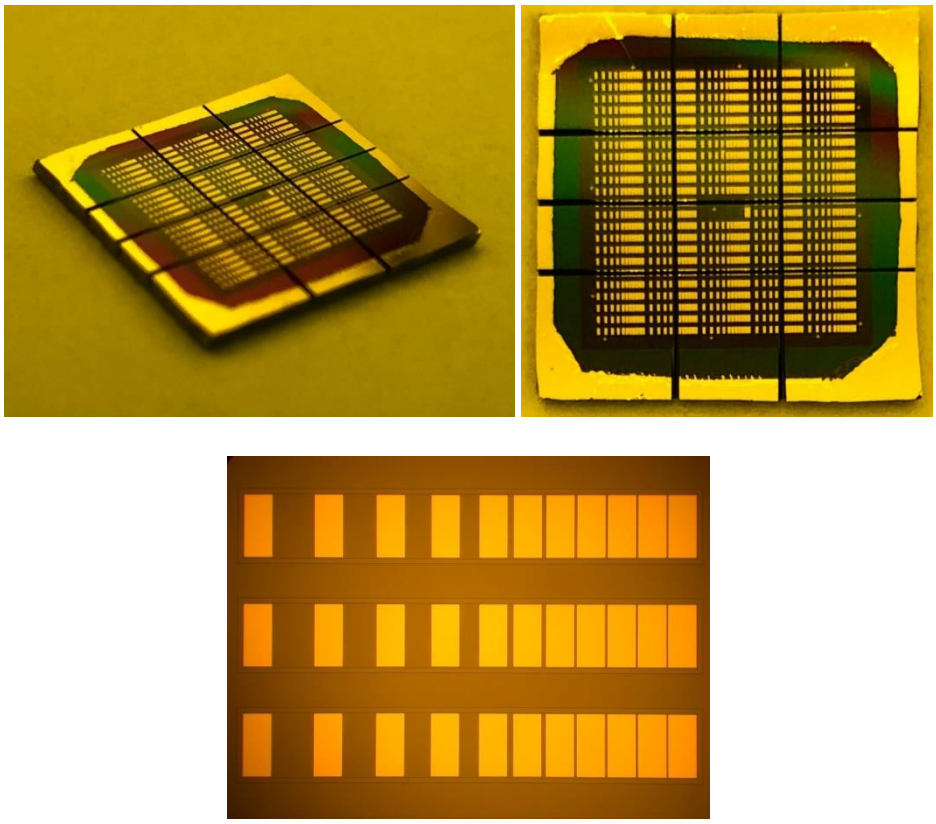

Figure 4.1. Transmission line measurement (TLM) samples prepared for annealing optimization.

As shown in Figure 4.2, two sets (two-step and three-step) of annealing profiles are illustrated. Both sets of profiles have an initial step at 450 °C for 3 minutes for stabilizing the equipment and avoiding power ramping overshooting. During this period samples can be heated up uniformly with no major interaction between the metal stack and (Al)GaN occurring. Afterwards for the two-step recipes, the temperature directly ramps up to high temperature and remains constant for 50 seconds, during which the interaction between the metal stack and (Al)GaN takes place and ohmic contacts are therefore formed. On the other hand, the three-step recipes have an additional step at 700 °C for 40 seconds, which is optimized as shown in Figure 4.3, before the high-temperature period. During this stage, Al diffusion toward GaN film is upgraded and Ti, Al and AlGaN/GaN can preliminarily react. Finally, the 30-second high temperature period boosts the reaction and allows ohmic contacts to form (Figure 4.4).

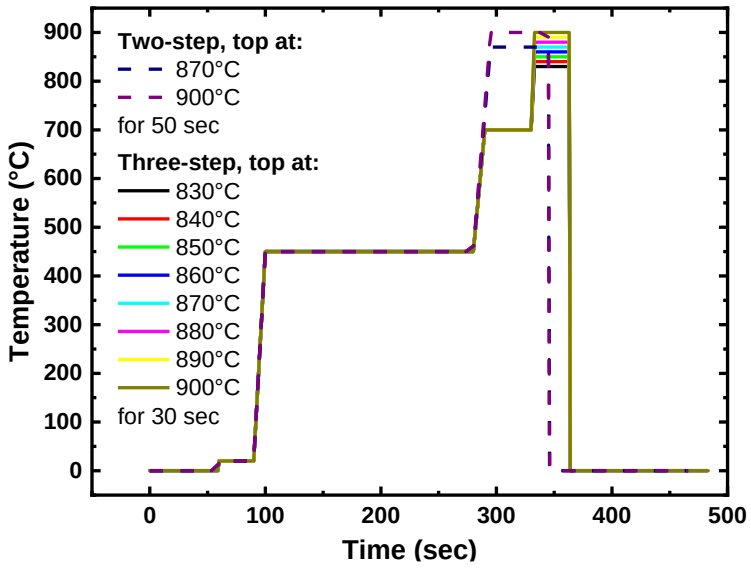

Figure 4.2. Rapid thermal annealing temperature profile. Two sets of annealing profiles are investigated for various levels of high temperature.

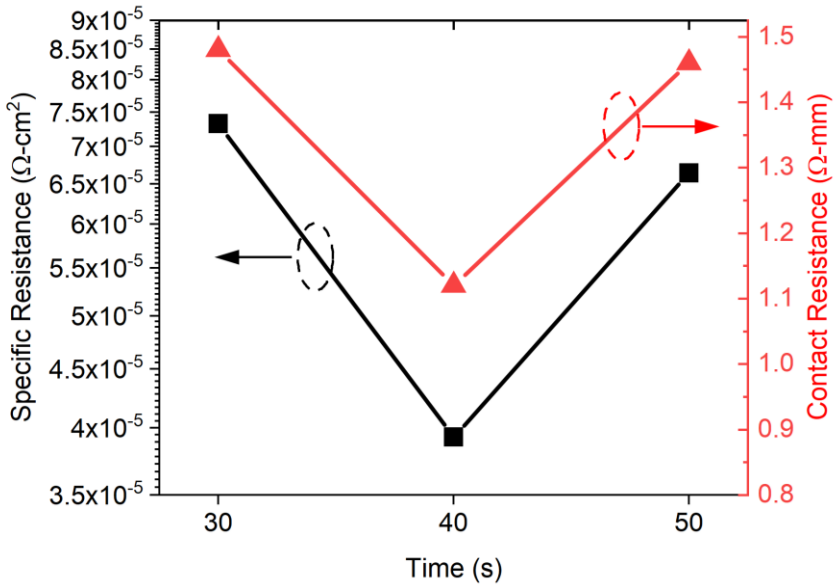

Figure 4.3. Time optimization for RTA step two. Step 1: at 450 °C for 3 min, Step 2: at 700 °C for 30, 40, and 50 sec, and Step 3: at 830 °C for 30 sec.

4.3 Results and conclusion

The results of contact resistance using the designed annealing profiles are shown in Figure 4.5 and Table 4.1. An ohmic metal contact with 4.3×10^{-6} Ω–cm^2 specific contact resistance and 0.28 Ω–mm contact resistance is achieved using three-step annealing recipe with high temperature at 900 °C for 30 second. A slightly improved contact is also achieved using three-step annealing recipe with high temperature at 900 °C for 40 second. For the two-step annealing process, it is observed that a higher temperature leads to a higher contact resistance, whereas for the three-step annealing process, a higher temperature leads to a lower contact resistance. It is suggested that a higher level of $AuAl_2$ formation could present at higher temperature given long enough time (50 second). However, given only 30 second at the high temperature, the formation of $AuAl_2$ is not as efficiently promoted by the increasing temperature. Instead, the increasing temperature promotes the formation of Ti and N and Ti and Al to form a better ohmic contact.

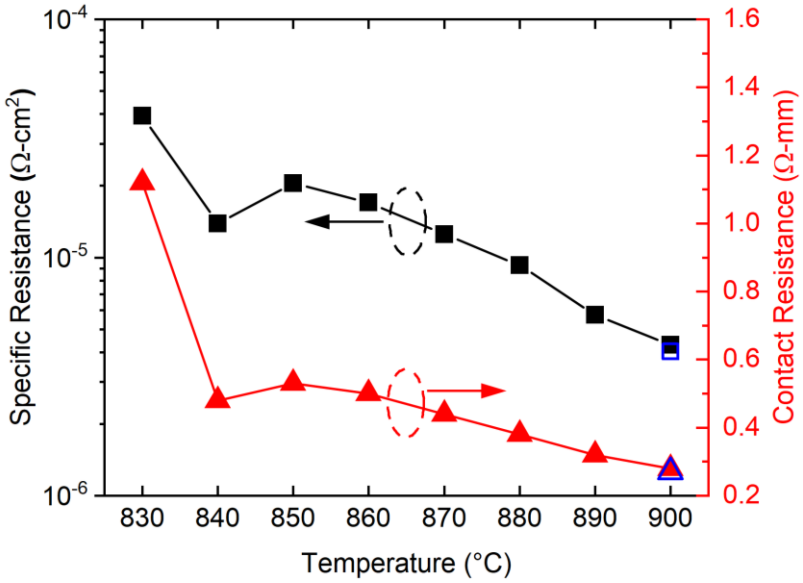

Figure 4.4. Temperature optimization for RTA step three. Step 1: at 450 °C for 3 min, Step 2: at 700 °C for 40 sec, and Step 3: at 830 ~ 900 °C for 30 sec

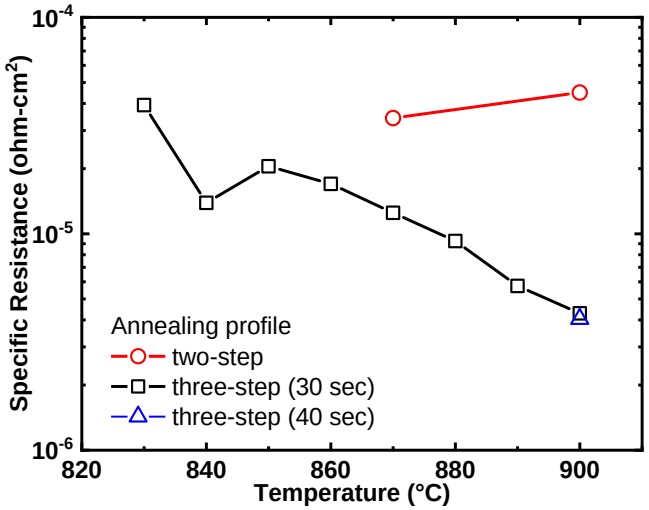

Figure 4.5. Measured contact resistances of samples annealed with the designed profiles. Three-step annealing recipes show lower contact resistance than the two-step annealing.

Table 4.1. Ohmic contact resistance obtained by using the designed annealing recipes. A metal contact with 4.04×10^{-6} Ω–cm^2 specific contact resistance and 0.27 Ω–mm contact resistance is achieved using three-step annealing recipe with high temperature 900 °C for 40 sec.

Annealing recipe	**Specific resistance**	**Contact resistance**
Two steps, high temperature at:		
870°C for 50 sec	3.423×10^{-5} Ω–cm^2	1.01 Ω–mm
900°C for 50 sec	4.495×10^{-5} Ω–cm^2	5.23 Ω–mm
Three steps, high temperature at:		
830°C for 30 sec	3.930×10^{-5} Ω–cm^2	1.12 Ω–mm
840°C for 30 sec	1.090×10^{-5} Ω–cm^2	0.42 Ω–mm
850°C for 30 sec	2.030×10^{-5} Ω–cm^2	0.53 Ω–mm
860°C for 30 sec	1.700×10^{-5} Ω–cm^2	0.50 Ω–mm
870°C for 30 sec	1.250×10^{-5} Ω–cm^2	0.44 Ω–mm
880°C for 30 sec	9.230×10^{-6} Ω–cm^2	0.38 Ω–mm
890°C for 30 sec	5.740×10^{-6} Ω–cm^2	0.32 Ω–mm
900°C for 30 sec	4.290×10^{-6} Ω–cm^2	0.28 Ω–mm
900°C for 40 sec	4.041×10^{-6} Ω–cm^2	0.27 Ω–mm

To further reduce the contact resistance, different metal stack configurations (material and thickness) need to be tested. In addition, different surface treatment methods before electron beam evaporation need to be tested to improve the quality of metal/(Al)GaN interface. Metal top surface condition should also be investigated in order to identify the tradeoff between contact resistance and surface roughness, as shown in Figure 4.6, among different recipes.

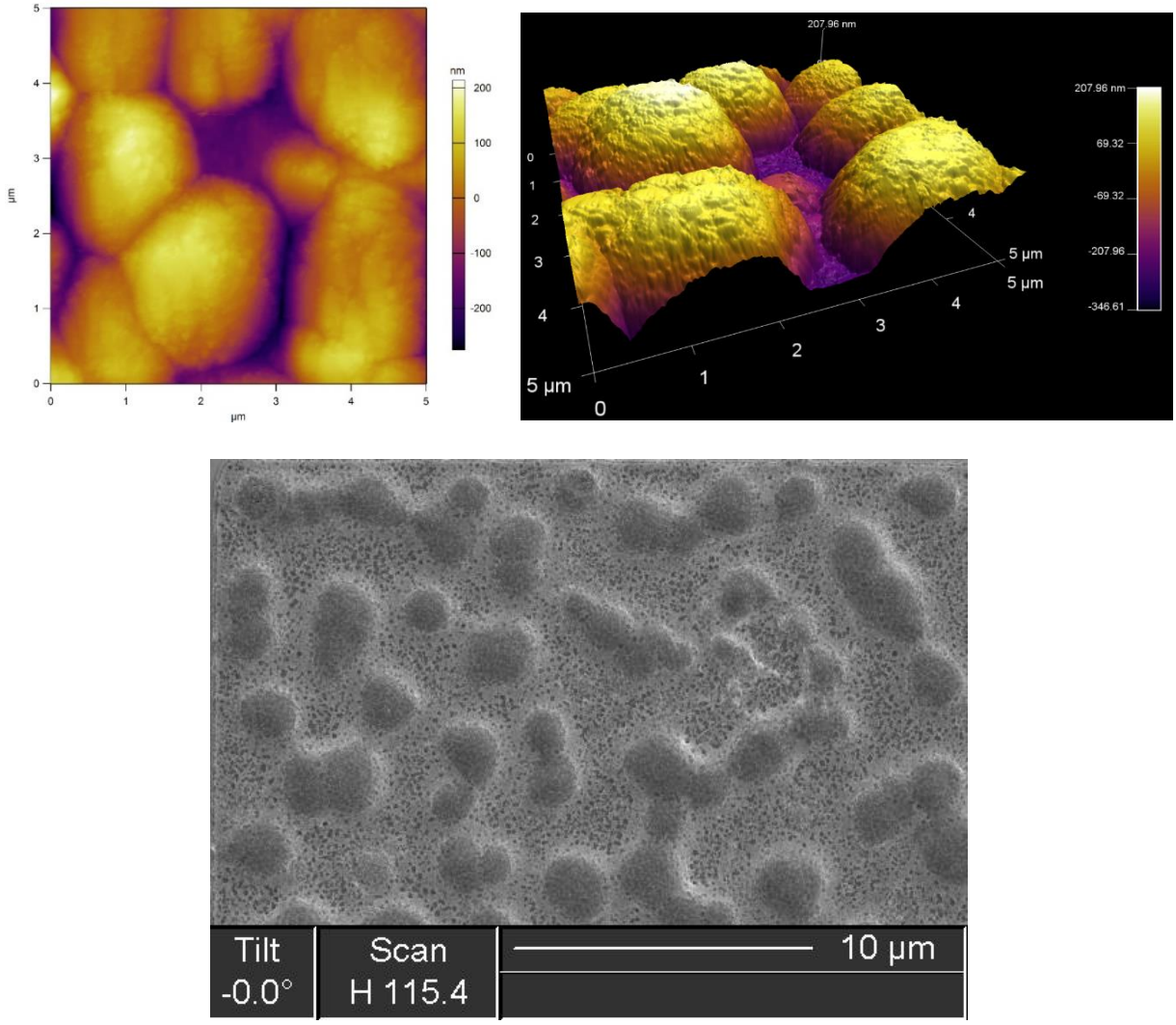

Figure 4.6. Surface morphology after RTA with the optimized recipe. The surface toughness after annealing is measured by AFM as 112 nm rms.

CHAPTER 5 IMPACT OF OHMIC CONTACT ANNEALING ON Al_2O_3/(Al)GaN INTERFACE TRAP STATE DENSITY AND GATE LEAKAGE CURRENT

Annealed, thin (~ 2.6 nm)-Al_2O_3/AlGaN/GaN metal-insulator-semiconductor (MIS) heterostructures on Si(111) are fabricated and studied via capacitance–voltage (C–V) measurements to quantify densities of fast and slow interface trap states and via current–voltage (I–V) measurements to investigate dominant gate current leakage mechanisms. Dual-sweep C–V measurements reveal small voltage hysteresis (~ 1 mV) around threshold voltage, indicating a low slow interface trap state density of ~ 10^9 cm^{-2}. Frequency-dependent conductance measurements show fast interface trap state density ranging from 8×10^{12} to 5×10^{11} $eV^{-1}cm^{-2}$ at energies from 0.275 to 0.408 eV below the GaN conduction band edge. Temperature-dependent I–V characterizations reveal that trap-assisted tunneling (TAT) dominates the reverse-bias carrier transport while the electric field across the Al_2O_3 ranges from 3.69 to 4.34 MV/cm, and the dominant Al_2O_3 trap state energy responsible for such carrier transport is identified as 2.13 ± 0.02 eV below the Al_2O_3 conduction band edge. X-ray photoelectron spectroscopy measurements on Al_2O_3 before and after annealing suggest an annealing-enabled reaction between Al-O bonds and inherent H atoms. Overall, we report that annealed, thin-Al_2O_3 dielectric is an effective (Al)GaN surface passivation alternative when minimizing passivation-associated parasitic capacitance is required, yet non-ideal for significantly suppressing gate leakage current in MIS structures due to the governing TAT carrier transport mechanism.

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5.1 Introduction

AlGaN/GaN high-electron-mobility transistor (HEMT) technology is the backbone of next-generation high-power and high-frequency electronics thanks to the high thermal and chemical stability and high critical electric fields of III-nitrides [4]. Emerging GaN-on-Si (111) technology platform further promises high-volume scalability of AlGaN/GaN HEMTs at low cost [14], [58]. Various dielectrics such as Al_2O_3, SiN_x, SiO_2 and HfO_2 are used as the insulator in metal-insulator-semiconductor (MIS) HEMTs or for (Al)GaN surface passivation in order to improve device performance. However, it is shown that the interface trap states at dielectric/(Al)GaN interfaces cause frequency-dispersive charging (trapping) and discharging (de-trapping) effects, leading to compromised reliability of AlGaN/GaN HEMTs [59], [60], [61], [62], [63], [64], [65], [66]; therefore, minimizing the density of interface trap states (D_{it}) is one of the most crucial tasks towards mature AlGaN/GaN HEMT technology. The density of interface trap states is sensitive to the choice of dielectric and how the dielectric was deposited. It has been reported that a high-quality dielectric/III–V interface can be achieved by Al_2O_3 (a high-κ dielectric) prepared by atomic layer deposition (ALD) thanks to high deposition uniformity and low inherit defect density [67], [68]. Nevertheless, processing challenges with AlGaN/GaN HEMTs, such as (Al)GaN surface treatment (prior to the dielectric deposition) and post-dielectric-deposition annealing (PDA) for ohmic contact formation, also profoundly affect D_{it} [69].

The impact of PDA on Al_2O_3/AlGaN/GaN MIS HEMT characteristics is an active research area. Benefits of employing PDA have indeed been reported, including improving Al_2O_3 properties that leads to reduced oxide traps and threshold voltage hysteresis [70] as well as reducing average D_{it} at the Al_2O_3/GaN interface [71]. Yet some studies report adverse effects [72], [73]. Further

systematic work is therefore needed for better understanding the impacts of PDA on ALD Al_2O_3 properties and then correlating these effects on AlGaN/GaN HEMT performance.

In this work, annealed, thin (~ 2.6 nm)-Al_2O_3/AlGaN/GaN MIS HEMT capacitors on Si(111) are fabricated and studied via capacitance–voltage (C–V) and current–voltage (I–V) measurements (by Keithley 4200A-SCS Parameter Analyzer). In particular, employing a thin Al_2O_3 layer is advantageous for both gate insulator and (Al)GaN surface passivation in MIS HEMTs. For gate insulator, a thinner layer allows a larger capacitance to better couple the applied electric field for controlling the channel while suppressing the gate leakage current (compared to a Schottky gate configuration) [12]. In addition, it has been reported that in highly scaled devices, fringing gate capacitance and drain-induced barrier lowering can be reduced with a thinner passivation, leading to a higher cutoff frequency and improved device performance [74]. Dual-sweep C–V and frequency-dependent conductance measurements are performed on the Al_2O_3/AlGaN/GaN MIS HEMT capacitors to quantify the densities of slow ($N_{it,slow}$) and fast interface trap states ($D_{it,fast}$), respectively. In addition, temperature-dependent I–V measurements are used to identify the dominant reverse-bias carrier transport across the thin Al_2O_3. Finally, X-ray photoelectron spectroscopy (XPS) measurements are carried out in order to compare the chemical compositions of as-deposited and annealed Al_2O_3 films.

5.2 Fabrication of Al_2O_3/AlGaN/GaN metal-insulator-semiconductor capacitors

By metal-organic chemical vapor deposition, the AlGaN/GaN HEMT structure is composed of AlGaN barrier layer (GaN capping layer / $Al_{0.23}Ga_{0.77}N$ barrier layer / AlN spacer layer, total thickness estimated as 13.7 nm by C–V measurements) / GaN channel layer, grown on a step-graded $Al_xGa_{1-x}N$ buffer layer stack composed of 240-nm-thick $Al_{0.30}Ga_{0.70}N$ / 210-nm-

thick $Al_{0.58}Ga_{0.42}N$ / 190-nm-thick $Al_{0.82}Ga_{0.18}N$ / 175-nm-thick AlN on a 200-mm Si(111). Room temperature ven dar Pauw Hall measurements determined two-dimensional electron gas (2DEG) sheet concentration and mobility as $8.9 \pm 0.1 \times 10^{12}$ cm^{-2} and 1802 ± 102 $cm^2/V\text{-}s$, respectively.

Using this material stack, Al_2O_3/AlGaN/GaN MIS HEMT capacitors are fabricated. The fabrication starts with surface degreasing (with toluene, acetone, methanol, de-ionized water) and surface treatment using 6% $HCl_{(aq)}$ at room temperature for 1 min, 7% $NH_4OH_{(aq)}$ at room temperature for 1 min, and 5% $(NH_4)_2S_{(aq)}$ at 50 °C for 30 min to remove organic contaminants, alkali ions, and native oxide. Then, 10-nm-thick Al_2O_3 is deposited via ALD for 100 cycles using precursors of H_2O and trimethylaluminum at 250 °C to serve as GaN surface passivation layer as well as a protection layer for the next processing steps. Mesa isolation is performed via wet etching of Al_2O_3 (by buffered oxide etching (BOE)) followed by dry etching of (Al)GaN (using Cl-based inductively coupled plasma reactive ion etching). Afterwards, the ohmic contact window is opened by Al_2O_3 wet etching using BOE, followed by metal deposition (Ti (20 nm) / Al (120 nm) / Ni (55 nm) / Au (45 nm)) using electron beam evaporation. A three-step (450 °C for 3 min, 700 °C for 40 s, and 900 °C for 40 s) rapid thermal annealing (RTA) is carried out in N_2 ambient and a specific ohmic contact resistance of 4.04×10^{-6} $\Omega\text{–}cm^2$ is achieved. The Al_2O_3 layer in the gate regions is then thinned by hot $HCl_{(aq)}$ for 1 min (remaining thickness estimated as 2.6 nm by C–V measurements), followed by the gate metal contact deposition (Ni (20 nm) / Au (200 nm)) using electron beam evaporation. Electrical measurements are then carried out. For comparison, AlGaN/GaN Schottky HEMT capacitors are also fabricated mostly in parallel with MIS ones except that Al_2O_3 in the gate regions is completely removed using BOE. Compared with the AlGaN/GaN Schottky HEMT capacitors, additional annealed 2.6-nm ALD Al_2O_3 in the MIS

HEMT capacitors results in approximately two orders of magnitude reduction in reverse-bias current density (Figure 5.1).

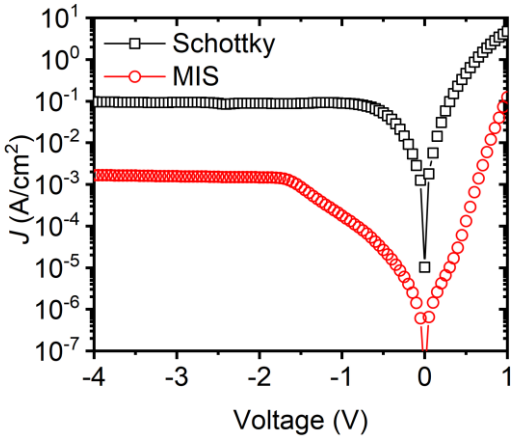


Figure 5.1. Gate leakage current densities of the Schottky and the MIS HEMT capacitors are provided. The annealed, thin (~ 2.6 nm) ALD Al_2O_3 in the MIS HEMT capacitor reduces the reverse-bias gate current density by approximately two orders of magnitude compared to that of the Schottky HEMT capacitor [57].

5.3 Characterization of density of interface trap states

Dual-sweep C–V measurements are first performed on the MIS HEMT capacitors to measure the hysteresis around the threshold voltages ($V_{T,MIS}$) in order to study $N_{it,slow}$ with time constant (τ_{it}) of tens of seconds at the Al_2O_3/GaN interface [75]. Such measurement typically serves as the first approach to preliminarily comprehend how the capacitor responds to the AC signal within the DC bias range, and the resulted hysteresis is one indicative factor. It is understood that hysteresis is associated with charging of interface trap states; therefore, it offers a measure to quantify the density of these interface trap states. Depending on the AC signal frequency and the up/down voltage sweeping rate, the density of a part of slow interface trap states can be estimated [76]. Electrical de-trapping is first performed by maintaining the gate voltage (V_G) at -4 V for 2 min, followed by applying a slow ramping DC bias at a speed of 0.05 V/s (first up-sweep and then down-sweep) superimposed with an AC signal at 100 kHz with 50 mV rms. The same

measurements are also performed on Schottky HEMT capacitors in order to extract capacitance ($C_{Schottky}$) and threshold voltage ($V_{T,Schottky}$) to be later used as inputs for determining the Al_2O_3 capacitance (C_{ox}) and Al_2O_3 electric field (E_{ox}) in the MIS HEMT capacitor. As shown in Figure 5.2 (a), the MIS HEMT capacitor exhibits sharp transitions from depletion into accumulation, indicating decent interface qualities. The threshold voltages ($V_{T,MIS}$ and $V_{T,Schottky}$) and C_{ox} are extracted as -1.58 V and -0.89 V, and 3088 nF/cm^2, respectively. During the dual sweep, when V_G is swept above $V_{T,MIS}$ (MIS HEMT capacitor is then pushed into accumulation) and then back to $V_{T,MIS}$, the energies of all the AlGaN/GaN interface trap states in the bandgap remain below the Fermi level; therefore, no change of occupancy in these interface trap states is expected. However, the energies of some of the Al_2O_3/GaN interface trap states in the bandgap are first pushed below (when V_G is swept up) and then again pulled above (when V_G is swept down) the Fermi level, hence the possibility of changing the occupancy [77]. In addition, at the sweeping speed of 0.05 V/s, the time needed to first sweep above $V_{T,MIS}$ and then back to $V_{T,MIS}$ is around 100 s; therefore, only the Al_2O_3/GaN interface trap states with τ_{it} longer than $100/2\pi$ s whose occupancy have also been altered during the measurement will contribute to the C–V hysteresis. According to the Shockley-Read-Hall (SRH) statistics

$$\tau_{it} = \frac{1}{v_{th}\sigma_{th}N_C}\exp\left(\frac{E_C - E_T}{kT}\right), \tag{5.1}$$

interface trap states with $\tau_{it} > 100/2\pi$ s correspond to energy levels with respect to the conduction band edge ($E_C - E_T$) > 0.81 eV at room temperature, where v_{th} (average thermal velocity of an electron), σ_{th} (trap state capture cross section) and N_C (effective density of states in the conduction band) are taken as 2×10^7 cm/s, 1×10^{-14} cm^2, and $4.3 \times 10^{14} \times T^{3/2}$ cm^{-3}, respectively [63], [73], [75], [78]. Given the voltage hysteresis (ΔV) extracted from the MIS HEMT capacitor (1 mV), the

$N_{it,slow}$ with $E_C - E_T > 0.81$ eV that also has altered occupancy in response to the dual sweeping is estimated as 3.33×10^9 cm^{-2} via

$$N_{\text{it,slow}} = C_{\text{MIS}} \times \frac{\Delta V}{q}, \tag{5.2}$$

where C_{MIS} is the total capacitance of the MIS HEMT capacitor in accumulation and q is elementary charge (1.6×10^{-19} C).

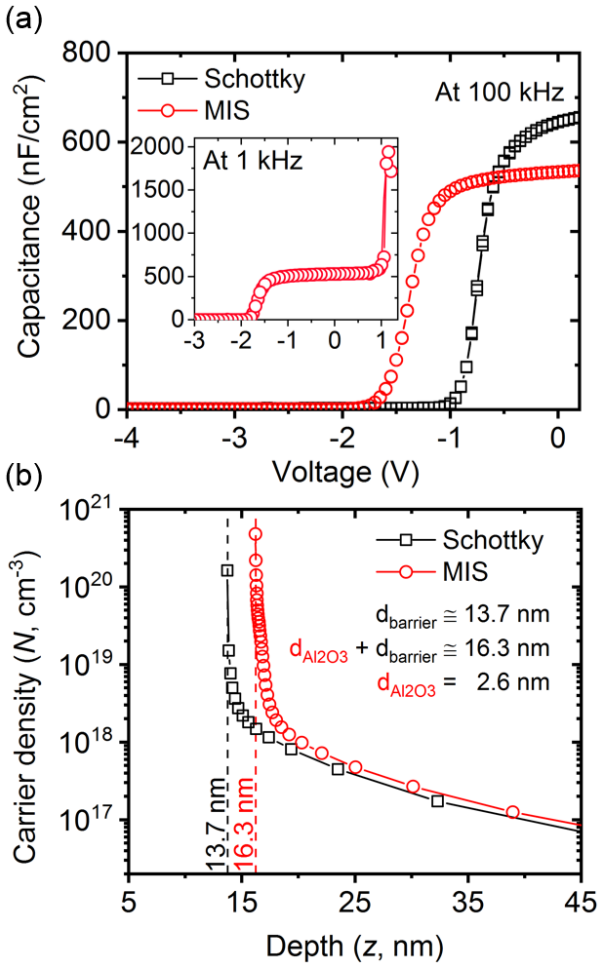
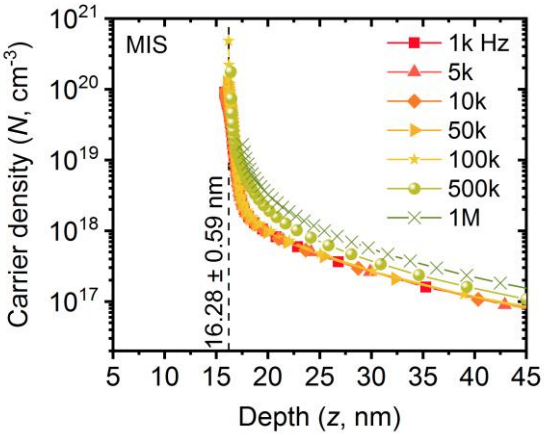


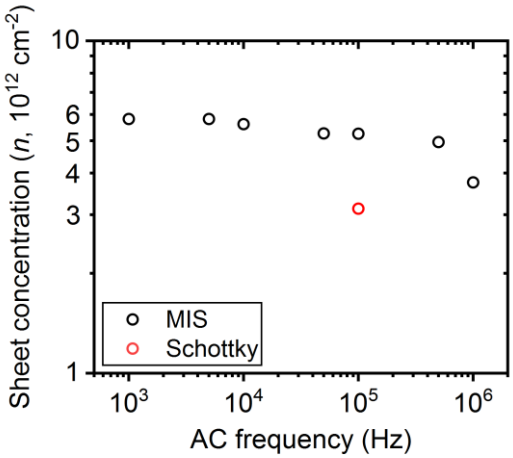
Figure 5.2. (a) Dual-sweep C–V plots of the AlGaN/GaN Schottky HEMT and Al_2O_3/AlGaN/GaN MIS HEMT capacitors. The inset shows the C–V characteristics of the MIS HEMT capacitor measured at 1 kHz. (b) Apparent carrier density obtained from the C–V characteristics of the two capacitors plotted as a function of depth [57].

It has also been reported that the hysteresis of a second capacitance increasing step in the forward bias region, associated with electrons in MIS HEMT capacitors out-spilling from the 2DEG channel and then accumulating at the Al_2O_3/barrier interface, can be used for analyzing $D_{it,fast}$ [63]; however, such method is not always feasible for MIS HEMT capacitors with thin insulator where the high forward bias leakage current can prohibit the appearance of such capacitance increase at elevated AC signal frequencies. The inset in Figure 5.2 (a) shows the C–V characteristics of the MIS HEMT capacitor measured at 1 kHz where the reduced capacitive admittance allows the appearance of the capacitance increase that is otherwise non-observable at 100 kHz. Even so, the capacitance still drops rapidly before reaching a constant value that corresponds to C_{ox}, negating the feasibility of reliably measuring the hysteresis for further $D_{it,fast}$ analysis. Therefore, other methods for probing $D_{it,fast}$ are required, such as the frequency-dependent conductance method.

On the other hand, apparent carrier density in the two capacitors as a function of depth is extracted from the 100 kHz C–V characteristics, as shown in Figure 5.2 (b). The peak positions approximately correspond to the 2DEG positions, and the shift between the two peaks indicates the thickness of the Al_2O_3 (d_{Al2O3}) in the MIS HEMT capacitor being approximately 2.6 nm [6], [63]. Integrating the apparent carrier density distribution over depth gives 2DEG sheet concentration of the MIS and Schottky HEMT capacitors being 5.25×10^{12} and 3.13×10^{12} cm^{-2}, respectively. In addition, the small frequency dispersion of 2DEG sheet concentration in the MIS HEMT capacitor (Figure 5.3) indicates a minor effect of series resistance in the structure [79].



(a)



(b)

Figure 5.3 (a) Frequency-dependent apparent carrier density distribution of the Al_2O_3/AlGaN/GaN MIS HEMT capacitor as a function of depth. The maximum carrier density location (~ 2DEG location) is 16.28 ± 0.59 nm with a small frequency dispersion [6], [63]. (b) 2DEG sheet concentration obtained by integrating the carrier density distributions over the depth [6]. The small frequency dispersion of 2DEG sheet concentration in the MIS HEMT capacitor indicates a small effect of series resistance in the structure [57], [79].

Frequency-dependent conductance method was originally developed for analyzing D_{it} in conventional MOSFETs [80], and it has also been widely adapted for GaN-based MIS HEMT interface analysis [60], [61], [77], [81], [82], [83], [84], [85]. This method measures the equivalent parallel conductance (G_p) that represents the power loss due to interface trap states capturing and emitting carriers as a function of V_G DC biasing and AC signal frequency (ω). Using this method, density of fast interface trap states with τ_{it} being around 0.1 to 100 µs is highlighted in this work.

During the measurements, the MIS HEMT capacitor is biased above $V_{T,MIS}$ in order to have unchanged occupancy of the AlGaN/GaN interface trap states in the bandgap [77]. The equivalent parallel conductance can be extracted using the measured parallel capacitance ($C_{p,meas}$), parallel conductance ($G_{p,meas}$), C_{ox}, and ω via the equation derived from MIS capacitor equivalent circuit model [60], [86]

$$G_p = \frac{\omega^2 C_{ox}^2 G_{p,meas}}{G_{p,meas}^2 + \omega^2 \left(C_{ox} - C_{p,meas}\right)^2}. \tag{5.3}$$

Then, $D_{it,fast}$ is extracted via fitting the normalized conductance G_p/ω as a function of ω at a given V_G, as shown Figure 5.4, using equation [80]

$$\frac{G_p}{\omega} = \frac{qD_{it,fast}}{2\omega\tau_{it}} \ln\left[1 + \left(\omega\tau_{it}\right)^2\right], \tag{5.4}$$

where τ_{it} further yields $E_C - E_T$ via Eqn. (5.1). Note that the measured G_P/ω increases towards lower frequencies, which necessitates an employment of a two-trap fitting model to better extract $D_{it,fast}$ [87]. As shown in Figure 5.5, the extracted $D_{it,fast}$ as a function of $E_C - E_T$ of the MIS HEMT capacitor is plotted along with the results from [75], [81], [88]. The highlighted $E_C - E_T$ ranging from 0.275 to 0.408 eV corresponds to $D_{it,fast}$ ranging from 8×10^{12} to 5×10^{11} $eV^{-1}cm^{-2}$, in line with the literature. In the literature, an order of magnitude lower $D_{it,fast}$ at the ALD Al_2O_3/GaN interface [81] compared to ours was reported (Figure 5.5), suggesting room for improvement in reducing $D_{it,fast}$ through Al_2O_3 ALD or RTA conditioning studies.

Though the frequency-dependent conductance method is widely used for extracting $D_{it,fast}$ in MIS HEMT structures [60], [61], [77], [81], [82], [83], [84], [85], it has also been suggested that using such method could render the $D_{it,fast}$ analysis in MIS HEMT structures inaccurate [89], [90]. Unlike in conventional MOSFETs, in MIS HEMT structures the dielectric/barrier interface trap states and the carriers in the channel are spatially separated by the barrier that has a gate-bias-

dependent resistance [89]. The presence of this resistive and capacitive barrier might post an artificial peak as large as $C_{Schottky}/q$ in the G_p/ω vs. ω plot, thereby producing a false $D_{it,fast}$ under certain conditions [90]. For instance, when the barrier is highly resistive, the main peak in the G_p/ω vs. ω plot that corresponds to the interface trap states may be pushed beyond the measurement frequency range, leaving the artificial peak misinterpreted as the main peak [90]. In this work, due to the relatively thin (13.7 nm) and thus low resistive barrier, $C_{Schottky}/q$ is approximately 4.0×10^{12} $eV^{-1}cm^{-2}$ whereas the extracted $D_{it,fast}$ corresponding to the peaks in the G_p/ω vs. ω plot mainly ranges from 10^{12} to 10^{13} $eV^{-1}cm^{-2}$. This suggests that in our work $D_{it,fast}$ is not being capped by the detection upper limit.

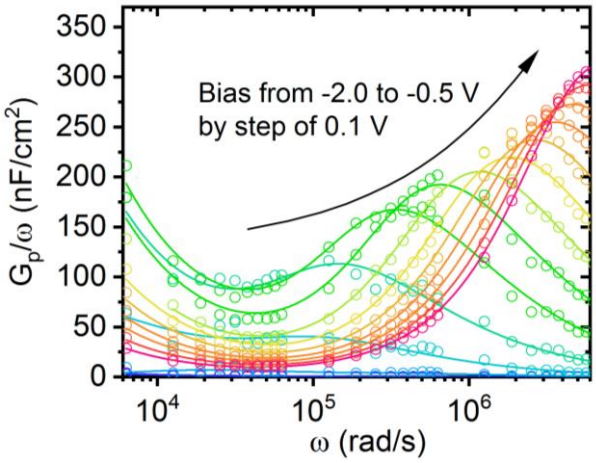


Figure 5.4. Frequency-dependent conductance plots of an Al_2O_3/AlGaN/GaN MIS HEMT capacitor as a function of bias from –2.0 to –0.5 V with a step of 0.1 V [57].

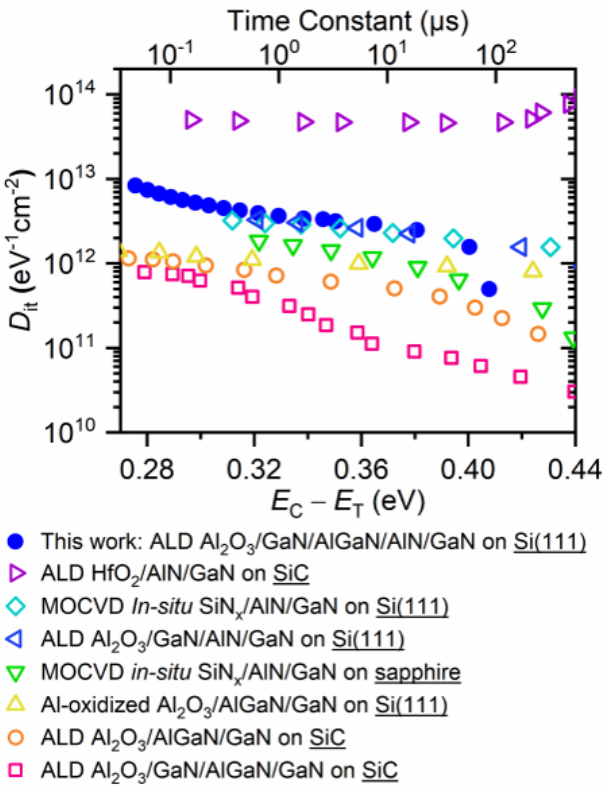


Figure 5.5. $D_{it,fast}$ as a function of the interface trap state energy levels for an Al_2O_3/AlGaN/GaN MIS HEMT capacitor [57].

5.4 Estimation of electric field and analysis of reverse-biased carrier transport

Gate leakage current analysis is used to study carrier transport mechanisms across insulators and thus evaluate the material quality. Common carrier transport mechanisms include trap-assisted tunneling (TAT), Poole-Frenkel (PF) emission, and Fowler-Nordheim (FN) tunneling [91], [92], [93], [94]. To distinguish the governing carrier transport mechanism, electric field across the insulator, in this work Al_2O_3 (E_{ox}), needs to be estimated first. Methods that involve different levels of complexity have been proposed to estimate E_{ox}. It is reported that the electric fields in the Al_2O_3 and the AlGaN barrier layers are considered identical and were estimated by using the concentrations of 2DEG and the sum of the polarization charges [92]. On the other hand, it was also proposed to consider the two electric fields separately and then estimate E_{ox} by

comparing the characteristics of Al_2O_3/AlGaN/GaN MIS HEMT capacitors and AlGaN/GaN Schottky HEMT capacitors [94], [95]. In this work, E_{ox} as a function of V_G is estimated via [95]

$$E_{ox} = \frac{Q - qn_{2DEG}}{\varepsilon_{ox}\varepsilon_0} \tag{5.5}$$

$$Q = C_{ox}\left(\frac{q\phi_B}{q} - \frac{\Delta E_C}{q} - \frac{qn_{polarization}}{C_{barrier}} - V_{T,MIS}\right) \tag{5.6}$$

$$\frac{qn_{polarization}}{C_{barrier}} = \phi_{Ni/GaN} - V_{T,Schottky}, \tag{5.7}$$

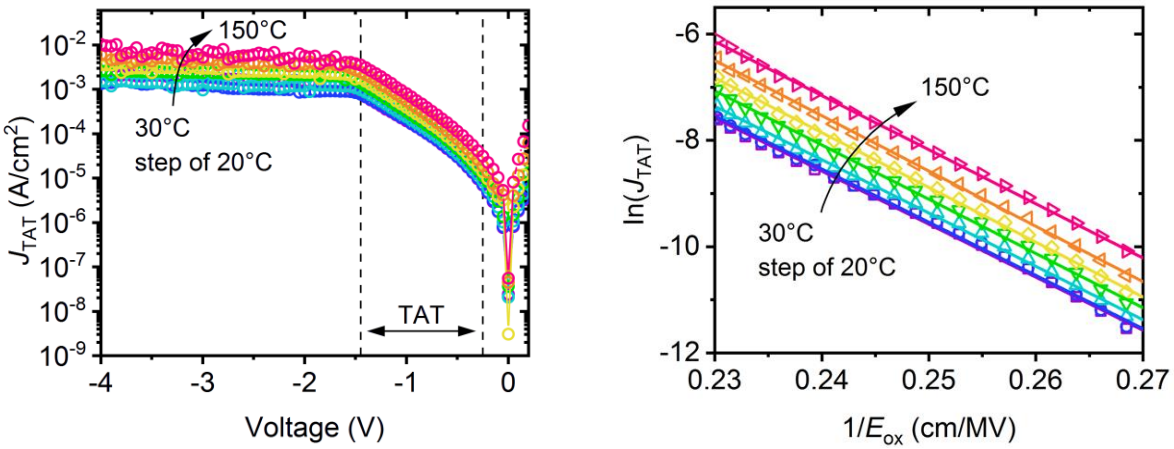
where n_{2DEG} is 2DEG sheet concentration as a function of V_G obtained from the MIS HEMT capacitor C–V measurement. ε_{ox}, ε_0, $q\phi_B$ (~ 3.5 eV) [96], $\phi_{Ni/GaN}$ (~ 0.95 eV) [95], and ΔE_C (~ 2.1 eV) [97] are relative permittivity of Al_2O_3, vacuum permittivity, Ni/Al_2O_3 barrier height, Ni/GaN Schottky barrier height, and Al_2O_3/GaN conduction band offset, respectively. $n_{polarization}$ is density of polarization charge. $C_{Schottky}$, C_{ox}, $V_{T,MIS}$, and $V_{T,Schottky}$ are 644 nF/cm^2, 3088 nF/cm^2, –1.58 V, and –0.89 V, respectively.

Reverse-bias carrier transport in the Al_2O_3/AlGaN/GaN MIS HEMT capacitors is then analyzed using temperature-dependent I–V characteristics, as shown in Figure 5.6 (a), as well as the estimated E_{ox}. In this bias region, carriers (electrons) are sent from the gate metal and then directly encounter the Al_2O_3, hence allowing a direct measure of the electrical property of the Al_2O_3 layer. Figure 5.7 schematically depicts electron transport across the Al_2O_3 via TAT, and the TAT current density (J_{TAT}) can be modeled as [91]

$$J_{TAT} \propto \exp\left(-\frac{8\pi\sqrt{2qm_{ox}^*}}{3hE_{ox}}\phi_T^{3/2}\right), \tag{5.8}$$

where h, m_{ox}* (Al_2O_3: 0.23m_e) [98], and $q\phi_T$ are Planck's constant, Al_2O_3 effective electron mass, and the trap energy relative to the conduction band edge, respectively. Slopes in ln(J_{TAT}) versus

$1/E_{ox}$ plot, as shown in Figure 5.6 (b), yield $q\phi_T$ as 2.13 ± 0.02 eV that exhibits a weak temperature dependence. In addition, the highlighted voltage region in Figure 5.6 (a) that fits the TAT model corresponds to E_{ox} ranging from 3.69 to 4.34 MV/cm, which is lower than the breakdown field of Al_2O_3 reported (5 to 10 MV/cm). Note that the increase in the reverse-bias current as a function of temperature can be explained by phonon-assisted TAT [99].



(a) (b)

Figure 5.6. (a) Temperature-dependent reverse-bias I–V curve plots of an Al_2O_3/AlGaN/GaN MIS HEMT capacitor. (b) Plot of ln(J_{TAT}) as a function of 1/E_{ox} at various measurement temperatures, indicating a trap state energy of 2.13 ± 0.02 eV [57].

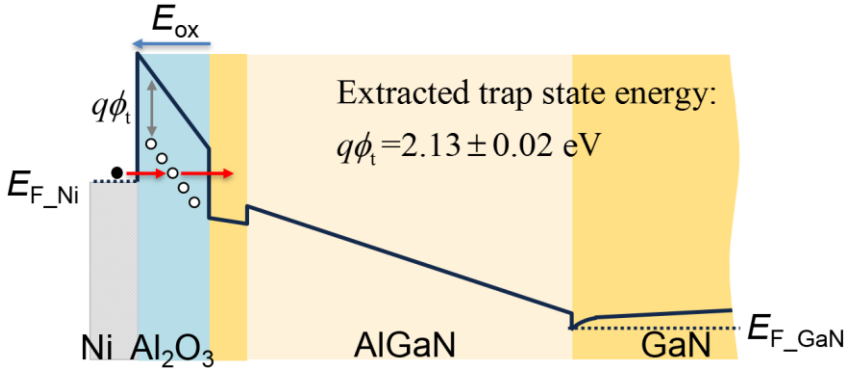


Figure 5.7. Sketch of the proposed trap-assisted tunneling carrier transport mechanism [57].

Other than TAT, PF emission is also a trap-related carrier transport mechanism where thermal fluctuation randomly promotes the trapped electrons in the insulator to the conduction band. These electrons will then momentarily propagate in the layer following the electric field before falling into another trap state. The current density (J_{PFE}) of such emission can be modeled as [91]

$$J_{PFE} \propto E_{ox} \times \exp\left[-\frac{q}{kT}\left(\phi_t - \sqrt{\frac{qE_{ox}}{\pi\varepsilon_{ox}}}\right)\right], \tag{5.9}$$

and slopes in $\ln(J_{PFE}/E_{ox})$ versus $E_{ox}^{0.5}$ plot (not shown here) yield $q\phi_T$ as 0.17 eV. The barrier height for electrons to overcome is therefore 3.33 eV ($q\phi_B - q\phi_T$); such a high barrier indicates that PF emission should not be a dominant reverse-bias carrier transport mechanism [92]. On the other hand, Fowler-Nordheim tunneling typically occurs at high electric fields where the barrier is in a triangular shape. The FN tunneling current density (J_{FNT}) can be modeled as [91]

$$J_{FNT} \propto E_{ox}^2 \times \exp\left[-\frac{8}{3}\frac{\pi\sqrt{2m_{ox}^*}}{qh}\frac{(q\phi_B)^{3/2}}{E_{ox}}\right], \tag{5.10}$$

and the slopes in $\ln(J_{FNT}/E_{ox}^2)$ versus $1/E_{ox}$ plot (not shown here) yield $q\phi_B$ (Ni/Al_2O_3 barrier height) as 2.0 eV, which is much smaller than the reported value 3.5 eV [96]. It is therefore considered that FN tunneling is not a dominant reverse-bias carrier transport mechanism in the selected bias range at temperatures above 30 °C.

5.5 X-ray photoelectron spectroscopy characterization

Before the ALD Al_2O_3 in the MIS HEMT capacitors is thinned by hot $HCl_{(aq)}$, it also goes through the high-temperature PDA with a maximum temperature at 900 °C for 40 sec known to alter the film property presumably due to microcrystallization [100]. Dielectric constants of as-deposited and annealed ALD Al_2O_3 are extracted from additionally fabricated Si-based metal-

oxide (Al_2O_3)-semiconductor capacitors as around 8 and 9 (~ 12.5% increase), respectively. During fabrication, the same three-step RTA condition is used. Determined by ellipsometry, the thickness of the Al_2O_3 film decreases by approximately 8.4% due to the RTA, in line with the previously reported trends [100]. Using the dielectric constant value of 9 and C_{ox} value of 3088 nF/cm^2, Al_2O_3 thickness in the Al_2O_3/AlGaN/GaN MIS HEMT is determined as 2.6 nm, agreeing with our earlier result in Figure 5.2 (b). Furthermore, other effects associated with PDA-enabled microcrystallization could include defect generation in the film and thus increased conductivity. To investigate the effect of high-temperature PDA on the ALD Al_2O_3 chemical composition, XPS measurements are further performed on as-deposited and annealed ALD Al_2O_3 with monochromatized Al Kα line (1486.61 eV) X-ray source. The obtained spectra are calibrated with respect to adventitious C 1s peak (284.8 eV) and then fitted with Gaussian – Lorentzian function where the full width at half maximum is restrained within 1.7 eV. As shown in Figure 5.8, the O 1s peaks in the two cases both reside at 531.1 eV, which correspond to the chemical state of Al_2O_3. The rather broad Al 2p peaks are then deconvoluted into two components that correspond to Al-O-H (74.1 eV) and Al_2O_3 (74.6 eV) chemical states [101]. The shown escalated Al-O-H component in the Al 2p peak after the PDA could be attributed to the PDA-enabled reaction between the Al-O bonds and the adjacent unbonded H residues/defects that inherently present in the ALD Al_2O_3 film, possibly coming from the chemical by-products of H_2O precursor and organic sources [102], [103]. Since it was reported that the conductivity of ALD Al_2O_3 is decreased upon dehydration that removes O-H [104], we suspect that the escalated Al-O-H component contributes to the dominating TAT carrier transport across the annealed Al_2O_3.

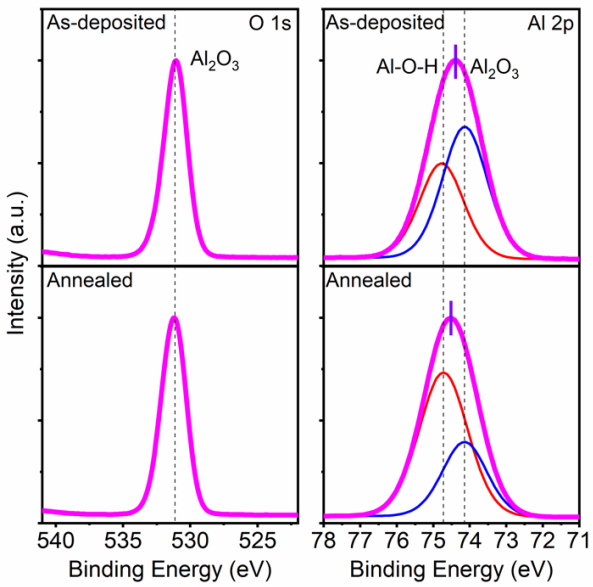


Figure 5.8. XPS measurements on as-deposited and annealed ALD Al_2O_3 [57].

5.6 Conclusion

Annealed, thin (~ 2.6 nm)-Al_2O_3/AlGaN/GaN MIS HEMT capacitors on a Si(111) substrate are fabricated and studied via C–V and I–V measurements to characterize $N_{it,slow}$, $D_{it,fast}$, and the dominant leakage mechanism associated with the annealed thin Al_2O_3. The small voltage hysteresis from the dual-sweep C–V measurement indicates low density of mobile ions and low $N_{it,slow}$ in the MIS HEMT capacitors, upholding the effectiveness of the GaN surface degreasing and treatment methods. The frequency-dependent conductance measurement shows that from 0.275 to 0.408 eV below the GaN conduction band edge, $D_{it,fast}$ at the Al_2O_3/GaN interface ranges from 8×10^{12} to 5×10^{11} $eV^{-1}cm^{-2}$, comparable with the literature results. Temperature-dependent I–V characterization reveals that TAT dominates the reverse-bias carrier transport across the annealed thin Al_2O_3 while E_{ox} ranges from 3.69 to 4.34 MV/cm, and the energy of the Al_2O_3 trap states responsible is extracted as 2.13 ± 0.02 eV below the Al_2O_3 conduction band edge. In addition, XPS suggests a PDA-enabled reaction between the Al-O bonds and the adjacent unbonded H

residues/defects that inherently present in the Al_2O_3 film due to the chemical by-products of H_2O precursor and organic sources. Such reaction is suspected to assist TAT in dominating the carrier transport across the annealed Al_2O_3. This work suggests that it is feasible to employ annealed thin ALD Al_2O_3 for effective (Al)GaN surface passivation, in order to reduce passivation-associated add-on parasitic capacitance, but not ideal for gate insulator for significantly suppressing leakage current due to the governing TAT carrier transport mechanism.

CHAPTER 6 SCHOTTKY-GATE AlGaN/GaN HEMT DC PERFORMANCE

Here we elaborate the Schottky-gate AlGaN/GaN HEMT DC performance. Note that the devices are simultaneously made with the AlGaN/GaN Schottky HEMT capacitors and Al_2O_3/AlGaN/GaN metal-insulator-semiconductor (MIS) HEMT capacitors analyzed in Chapter 5. The fabricated Schottky-gate AlGaN/GaN HEMT can be visualized in Figure 6.1 and Figure 6.2.

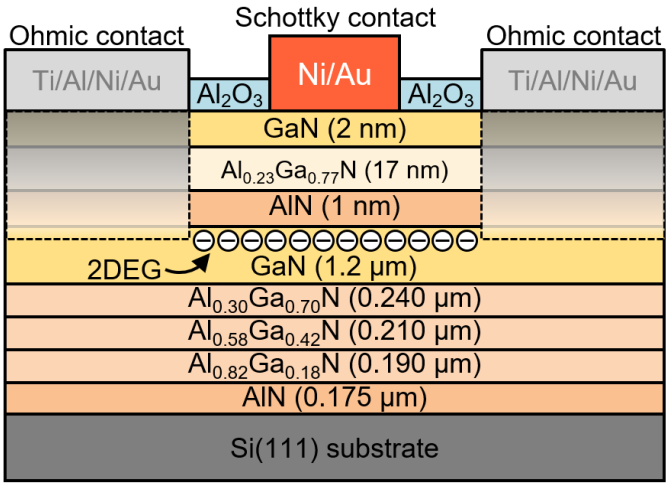


Figure 6.1. Schematic cross section diagram of the Schottky-gate AlGaN/GaN HEMTs.

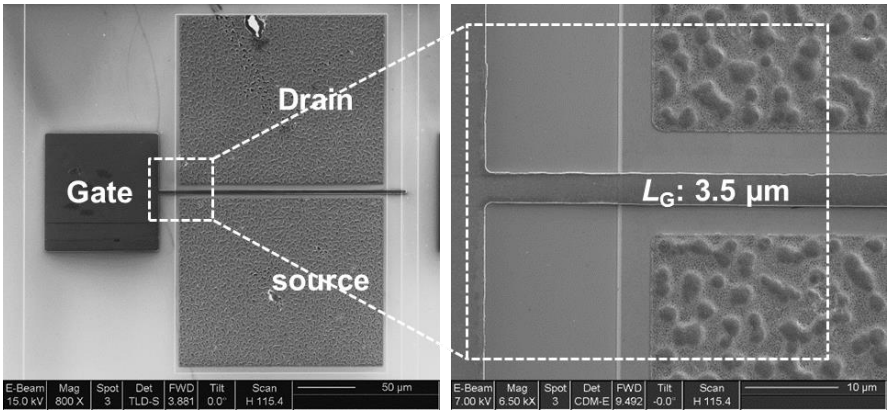


Figure 6.2. SEM top view image of the Schottky-gate AlGaN/GaN HEMTs.

6.1 Electrical measurement, analysis, and conclusion

DC I–V characteristics of a 3.5 µm Schottky gate AlGaN/GaN HEMT are analyzed. As shown in Figure 6.3, threshold voltage (V_T) is extracted as -0.87 V from $I_D^{0.5}$–V_{GS} relation at V_{DS} = 3.5 V, which, to our knowledge, is higher than most of the normally-on AlGaN/GaN HEMT devices reported to date. Due to the nature of spontaneous and piezoelectric polarizations (P_{SP} and P_{PE}) of wurtzite (Al)GaN materials, conventional AlGaN/GaN HEMTs are normally-on (depletion mode) devices, and the reported V_T have been mostly below –3 V [13], [95], [105], [106], [107]. Only a few with –2 V < V_T < –1.5 V have been reported to date [13], [108]. For a normally-on device, a higher V_T allows a lower supply voltage for operation, hence is more beneficial for reducing power consumption. As shown in Figure 6.4, A $g_{m,max}$ of 131.67 mS/mm is also extracted at V_{DS} = 3.5 V.

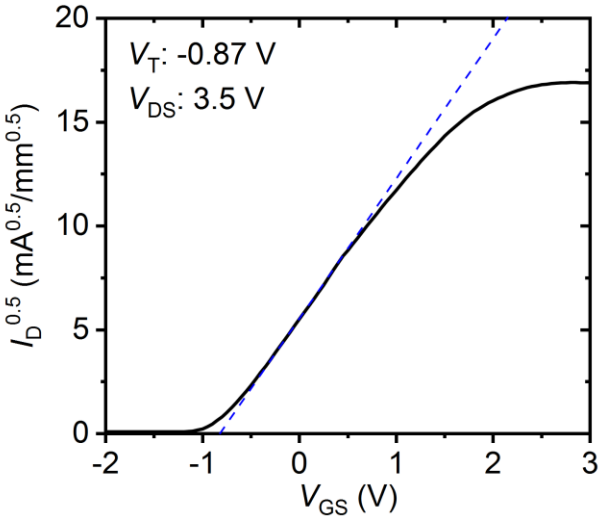


Figure 6.3. Threshold voltage extraction from $I_D^{0.5}$ – V_{GS} plot.

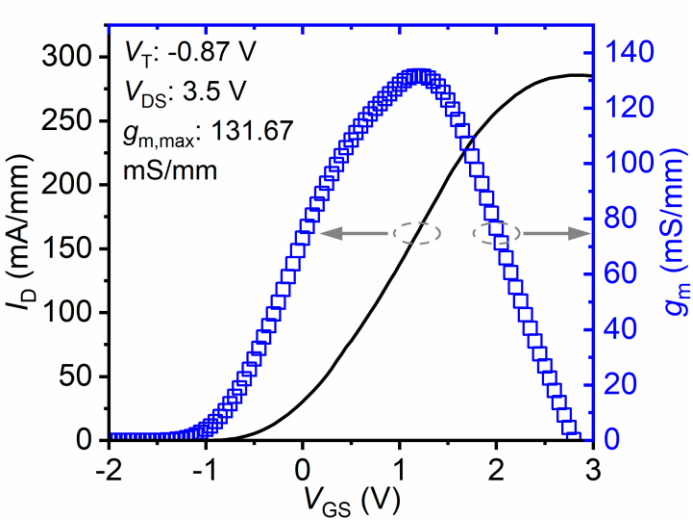


Figure 6.4. I_D – V_{GS} plot and the extracted g_m.

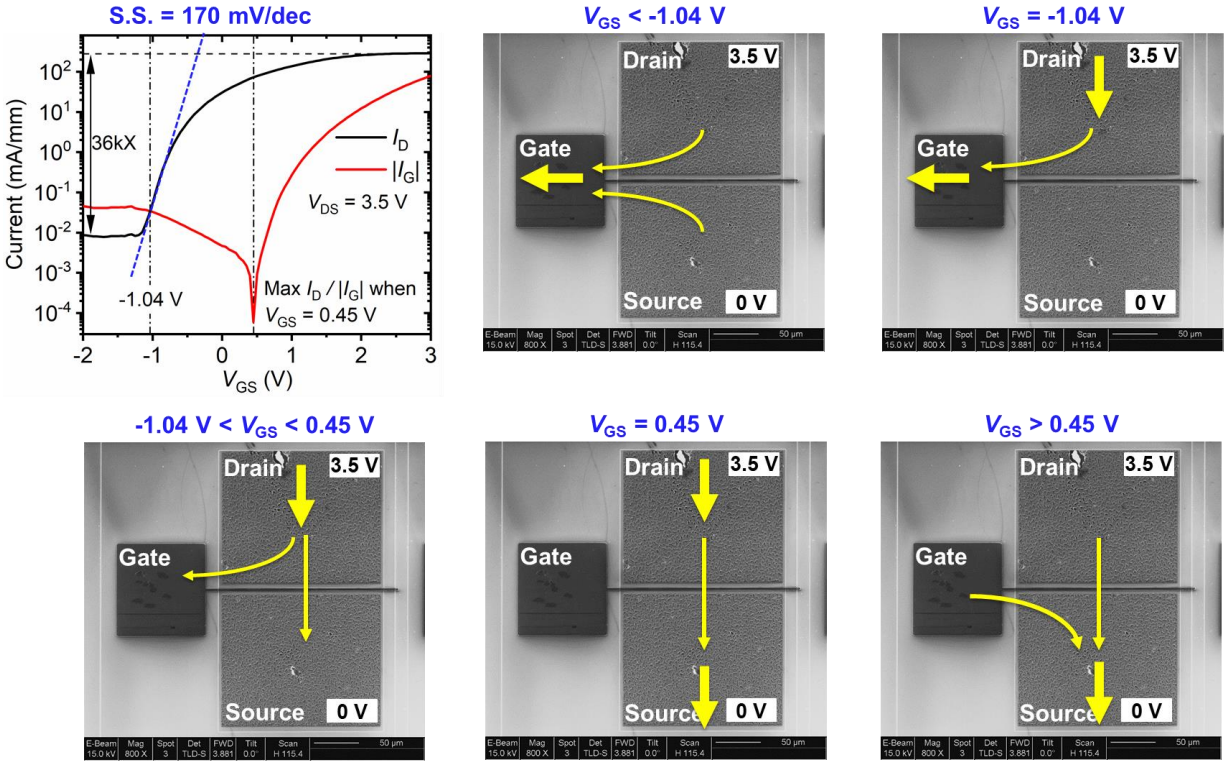


Figure 6.5. I_D/I_G – V_{GS} plot and net current flow analysis.

Characteristics of I_D and $|I_G|$ at V_{DS} = 3.5 V as a function of V_{GS} are then shown in Figure 6.5. I_D exhibits an on/off ratio of 36k and I_G has a minimum value at V_{GS} = 0.45 V. $|I_G|$ exceeds I_D when V_{GS} < -1.04 V, which means that electrons are supplied from gate to both drain and source. When V_{GS} = -1.04 V, I_D becomes equal to $|I_G|$ where all electrons from the gate are sent to drain side (source current is then zero). Once V_{GS} exceeds -1.04 V, more electrons from the source start to leak out and reach to drain via the channel (subthreshold region). The decrease of $|I_G|$ and rapid increase of I_D when -1.04 V < V_{GS} < 0.45 V suggest that most electrons the drain receives are from the source via the channel turned on by V_{GS}. After reaching a maximum value of I_D / $|I_G|$ at V_{GS} = 0.45 V, electrons from the source not only flow to the drain but also leak out to the gate; in other words, the gate is competing with the drain for electrons. The rapidly increasing $|I_G|$ limits the further increase of I_D and therefore on/off ratio. On the other hand, a decent pinch-off characteristic is observed with V_{DS} biased at least up to 10 V, as shown in Figure 6.6.

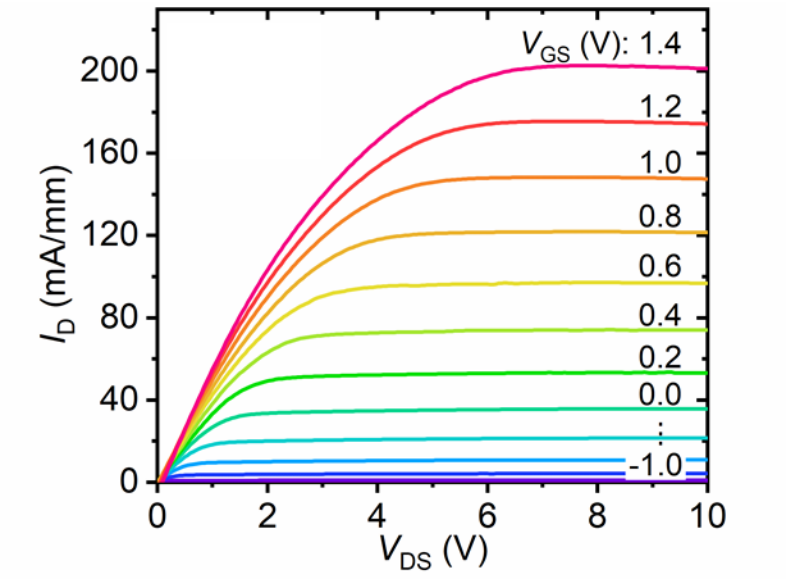


Figure 6.6. I_D – V_{DS} family curve. Decent pinch-off behavior can be observed up to V_{DS} = 10 V.

Figure 6.7 demonstrates the conducting characteristics of access and channel regions in the AlGaN/GaN HEMTs. Total resistance (source/drain contacts + access + channel) of symmetric AlGaN/GaN HEMTs with various lengths of $L_{GD} + L_{GS}$ is extracted from measured $I_D - V_{DS}$ curves at V_{DS} = 10 mV where the devices are working in the linear region, as shown in Figure 6.7 (a). The slopes of the fitted lines are used to calculate sheet resistance (R_S) of the access region as 476.62 ± 62.60 Ω/□. The sheet resistance of the channel region as a function of V_{GS} can then be extracted using the y-intercept of each fitted line while knowing $R_{contact}$ (33.44 Ω) that is calculated by comparing measurement results of devices with various geometries. As shown in Figure 6.7 (b), R_S of the access region remains constant while that of the channel region decreases as a function of V_{GS}.

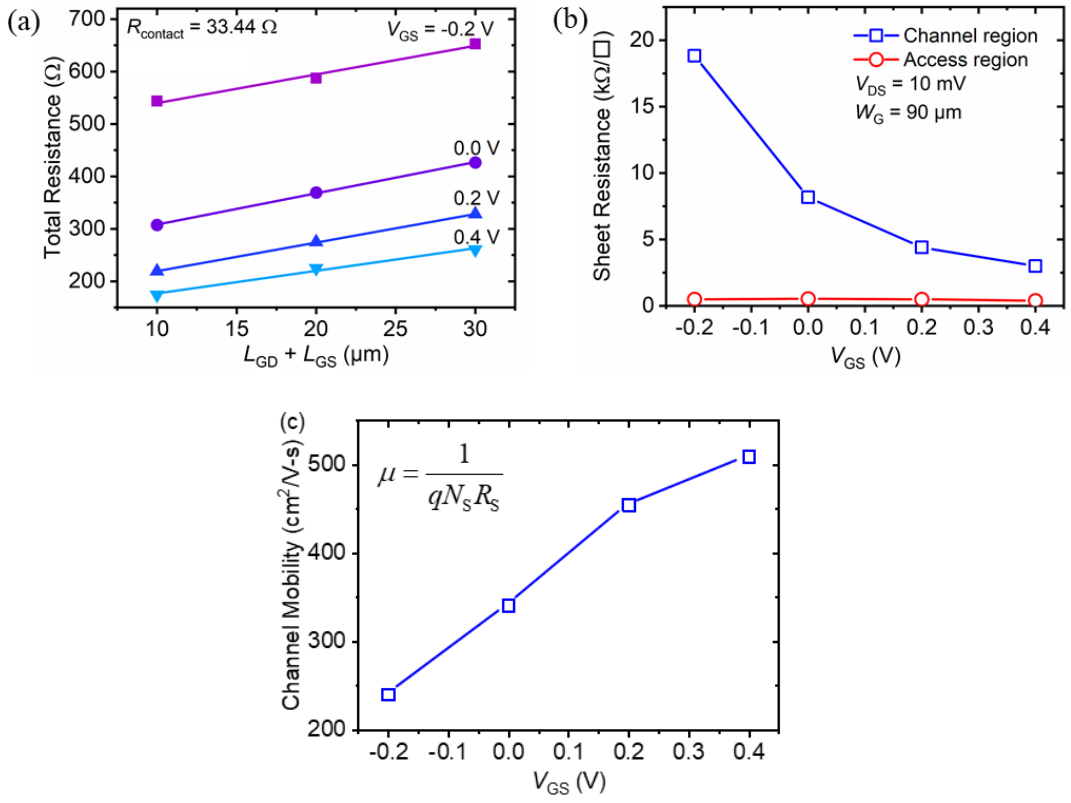


Figure 6.7. Characteristics of access and channel regions. (a) Total resistance (contacts + access + channel) of AlGaN/GaN HEMTs as a function of $L_{GD} + L_{GS}$ at V_{DS} = 10 mV and (b) the extracted R_S of the access and channel regions. (c) Channel mobility as a function of V_{GS}.

Given the high Schottky-gate leakage behavior, the effective Schottky gate barrier height at the Ni/GaN junction is additionally investigated using temperature-dependent reverse-biased I–V measurements on the AlGaN/GaN Schottky HEMT capacitor, as shown in Figure 6.8 (a). An Arrhenius plot of reverse-biased I_G is shown in Figure 6.8 (b). For a metal-semiconductor contact, I–V relation can be modeled by thermionic emission equation [109]

$$I_G = AA^*T^2 \exp\left(-q\phi_b / kT\right)\left\{\exp\left(qV_G / kT\right)-1\right\}, \tag{6.1}$$

where A is area, A^* is Richardson constant, T is temperature, $q\phi_b$ is effective barrier height at Ni/GaN junction, and k is Boltzmann constant. If $V_G < -3kT/q$, the equation can be approximately rearranged as

$$\ln\left(-\frac{I_G}{T^2}\right) = \ln\left(AA^*\right) - \frac{q\phi_b}{kT}, \tag{6.2}$$

where $q\phi_b$ can be extracted accordingly from the Arrhenius plot as a function of V_G, as shown in Figure 6.8 (c). The reported theoretical Schottky barrier height of Ni/GaN is 0.95 eV [110]; however, due to the existence of conductive dislocation-related continuum states [111], the extracted effective barrier height is only approximately 0.3 eV when V_G approaches 0 V, which is in line with several previously reported values [112], [113], [114], [115]. The effective barrier height first decreases when V_G is biased more negatively. When $V_G < -1$ V, $q\phi_b$ remains at minimum and $|I_G|$ is therefore kept saturated. In this bias region, neither I_G or $q\phi_b$ is controlled by V_G.

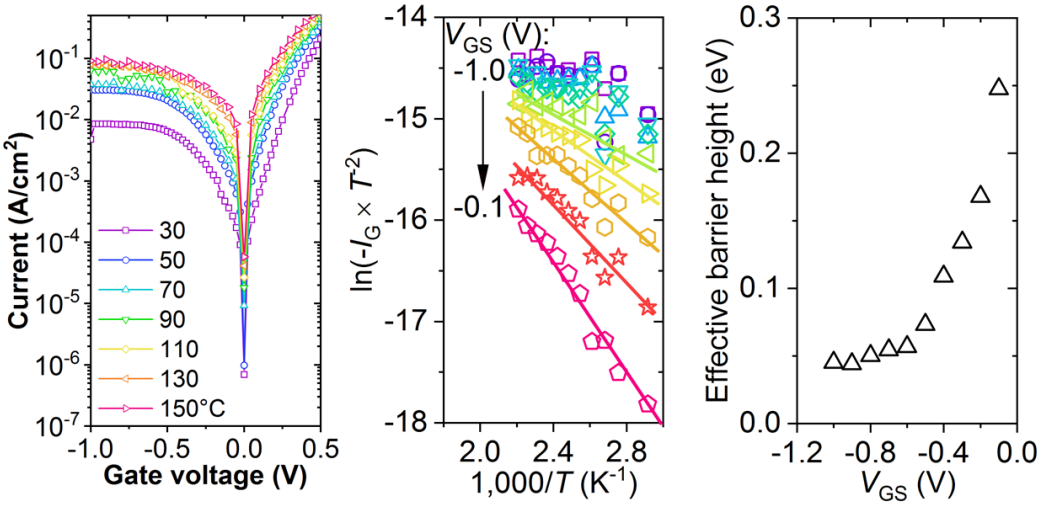


Figure 6.8. Effective Ni/GaN Schottky barrier height investigation. (a) Temperature-dependent I-V measurement on an AlGaN/GaN Schottky HEMT capacitor. (b) Arrhenius plot of reverse-biased gate current. (c) Extracted effective Schottky barrier height as a function of V_{GS}.

CHAPTER 7 IMPROVING CURRENT ON/OFF RATIO AND SUBTHESHOLD SWING OF SCHOTTKY-GATE AlGaN/GaN HEMTS BY POST-METALLIZATION ANNEALING

Al_2O_3-passivated Schottky-gate AlGaN/GaN HEMTs with improved subthreshold swing and drain current on/off ratio by post-metallization annealing at 500 °C in N_2 ambient are reported. With the post-metallization annealing, the gate leakage current in the reverse biased region and off-state drain current are reduced by more than three orders of magnitude, leading to a low subthreshold swing of 84.75 mV/dec and a high drain current on/off ratio of 2.1×10^7. Through temperature-dependent current-voltage measurements on dual Schottky gate structures and capacitance-voltage measurements on Al_2O_3/AlGaN/GaN MISHEMT capacitors, it is identified that the post-metallization annealing greatly suppresses both the Al_2O_3/AlGaN interface leakage current and the reverse gate leakage current by eliminating Al_2O_3/AlGaN interface trap states with 0.34 eV trap state energy and changing the dominant mechanism of reverse gate leakage conduction from trap-assisted tunneling to Fowler–Nordheim tunneling, respectively. Overall, this work reports on the effectiveness of post-metallization annealing in improving the performance of Schottky-gate AlGaN/GaN HEMTs and the underlying improving mechanisms.

7.1 Introduction

AlGaN/GaN high-electron-mobility transistors (HEMTs) are of great interest for the next-generation high-frequency and high-power electronics, thanks to III-nitride materials' high chemical and thermal stabilities, high critical electric field, and high electron saturation velocity

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[4]. In particular, the wurtzite phase materials' polarization effects allow formations of 2-D electron gas (2DEG) with high mobility to be utilized as conducting channel. Hindered by the high cost of native substrates, epitaxially growing (Al)GaN materials on foreign substrates is currently the mainstream approach, and integrating (Al)GaN on Si(111) further promises high volume scaling for cost reduction [14], [58].

Among various transistor specifications, drain current ON/OFF ratio ($I_{D,ON/OFF}$) and subthreshold swing (*S.S.*) are two figures of merit that emphasize the device efficiency and controllability. For Schottky-gate AlGaN/GaN HEMTs, the OFF-state drain current ($I_{D,OFF}$) often correlates closely with the gate leakage current due to lack of additional insulating material under the gate metal. In addition, it has also been reported that a lower gate leakage current leads to a superior *S.S.* [116]. Therefore, various approaches have been adapted to excel the performance of Schottky-gate AlGaN/GaN HEMTs in these regards. Oxide-filled isolation with N_2/H_2 post-gate annealing was proposed to suppress $I_{D,OFF}$ and then improve $I_{D,ON/OFF}$ [117]. Inserting p-InGaN on AlGaN barrier followed by a chlorine-based try etching was also proven beneficial for achieving a high $I_{D,ON/OFF}$ and a low *S.S.* [118]. On the other hand, post-metallization annealing (PMA), a simple yet effective method, has been utilized to tailor oxide/III-nitride interface property [119] and to reduce $I_{D,OFF}$ in Al_2O_3/GaN/AlGaN/GaN MISHEMTs [120], [121]. As effective as PMA is, more studies are nevertheless still needed to help better understand the underlying improving mechanisms.

In this work, we revisit the effect of PMA particularly on the performance of Schottky-gate AlGaN/GaN HEMTs with Al_2O_3 passivation in the access regions. With PMA, reverse gate leakage current and leakage current that flows from drain via the Al_2O_3/AlGaN interface to gate are significantly suppressed. Note that the reverse gate leakage current here specifically refers to

the leakage current that flows across the AlGaN barrier from the 2DEG channel to the gate that is reversely biased. As a result, both gate leakage current in the reverse biased region and $I_{D,OFF}$ are reduced by more than three orders of magnitude, leading to an $I_{D,ON/OFF}$ of 2.1×10^7 and an *S.S.* of 84.75 mV/dec. Mechanisms of the reverse gate leakage and Al_2O_3/AlGaN interface conduction, with and without PMA, are investigated and correlated with Al_2O_3/AlGaN interface trap states.

7.2 Device fabrication

Grown by metal organic chemical vapor deposition, the AlGaN/GaN HEMT structure is composed of 13.7-nm-thick AlGaN barrier layer (GaN cap / $Al_{0.23}Ga_{0.77}N$ barrier / AlN spacer) / 1200-nm-thick GaN layer on a step-graded buffer layer stack (240-nm-thick $Al_{0.30}Ga_{0.70}N$ / 210-nm-thick $Al_{0.58}Ga_{0.42}N$ / 190-nm-thick $Al_{0.82}Ga_{0.18}N$ / 175-nm-thick AlN) on Si(111) [57].

Two samples are then prepared using the material stack for studying the effect of PMA. Mesa isolation is first performed using Cl-based inductively coupled plasma reactive ion etching, followed by deposition of Ti (20 nm) / Al (120 nm) / Ni (55 nm) / Au (50 nm) by electron beam evaporation for forming ohmic contacts. To form ohmic contacts, a three-step rapid thermal annealing in N_2 ambient is then performed (450 °C for 3 mins, 700 °C for 40 s, and then 900 °C for 40 s), leading to a specific contact resistance of 5.3×10^{-6} Ω−cm^2. 20-nm-thick Al_2O_3 is deposited via atomic layer deposition at 250 °C, followed by selective removal of Al_2O_3 by buffered oxide etching (BOE) in order to expose GaN surface for surface treatments (6% $HCl_{(aq)}$ at room temperature (RT) for 1 min, 7% $NH_4OH_{(aq)}$ at RT for 1 min, and then 5% $(NH_4)_2S_{(aq)}$ at 50 °C for 30 mins), while the ohmic contacts are protected by the remaining Al_2O_3. Then, 10-nm-thick Al_2O_3 is deposited as gate oxide for metal-insulator-semiconductor (MIS) HEMT structures and for AlGaN/GaN HEMT surface passivation. Deposition of gate contacts (Ni (20 nm) / Au (200 nm)) by electron beam evaporation completes the MIS HEMT structures, whereas for Schottky-

gate HEMT structures, removal of Al_2O_3 in the gate region is performed prior to gate contact deposition. Finally, the Al_2O_3 that covers the ohmic contacts is removed by BOE. Till this point, one sample is kept as is while the other one receives PMA at 500 °C in N_2 ambient for 10 min.

7.3 Result and discussion

The Schottky-gate AlGaN/GaN HEMTs used for electrical characterization are with 2-μm gate length (L_G), 180-μm gate width (W_G), 2-μm gate-to-source distance, and 13-μm gate-to-drain distance. Figure 7.1 shows the comparisons of I_D and $|I_G|$ as a function of V_{GS}, with and without PMA. Without PMA, the Schottky-gate AlGaN/GaN HEMT suffers from high $|I_G|$ in the reverse biased region, high $I_{D,OFF}$, and low $I_{D,ON}$, resulting in a low $I_{D,ON/OFF}$ of 1.2×10^2 and a very large *S.S.* of 1014 mV/dec. With PMA, the device performance is drastically improved. $|I_G|$ in the reverse biased region and $I_{D,OFF}$ are both reduced by more than three orders of magnitude, and $I_{D,ON}$ has also been improved by one order of magnitude. As a result, a high $I_{D,ON/OFF}$ of 2.1×10^7 and a small *S.S.* of 84.75 mV/dec are achieved with the Schottky-gate AlGaN/GaN HEMT.

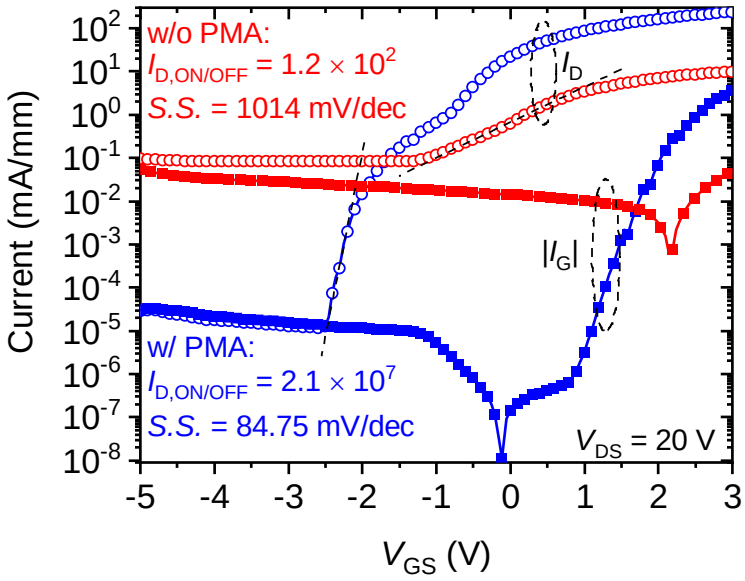

Figure 7.1. Comparisons of I_D and $|I_G|$ as a function of V_{GS}, with and without PMA.

Figure 7.2 reveals the DC output characteristics of the Schottky-gate AlGaN/GaN HEMT with PMA. From $I_D - V_{GS}$, threshold voltage (V_T) and maximum transconductance ($g_{m,max}$) are extracted as −0.92 V and 78.88 mS/mm, respectively. The relatively high V_T and the fact that the $g_{m,max}$ corresponds to a positive value of V_{GS} could be attributed to the relatively thin AlGaN barrier (~13.7 nm) in the structure. $I_D - V_{DS}$ also shows a decent pinch-off behavior with noticeable current collapse at V_{GS} = 1.5 V.

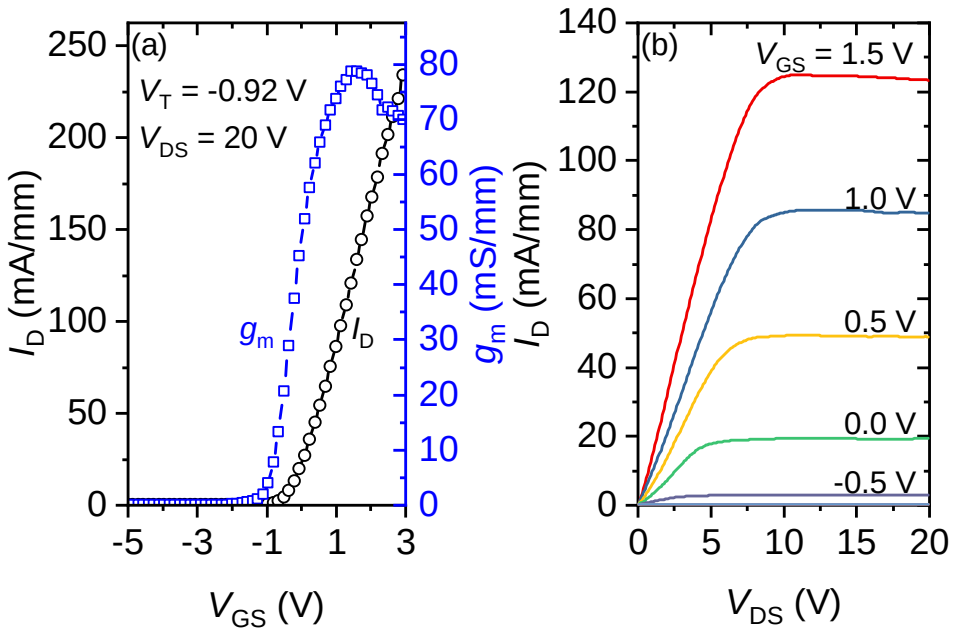

Figure 7.2. DC output characteristics of the Schottky-gate AlGaN/GaN HEMT with PMA. (a) $I_D - V_{GS}$, (b) $I_D - V_{DS}$.

In order to highlight the effects of PMA on individual leakage components, dual Schottky gate structures that are simultaneously fabricated along with the HEMTs, as shown in Figure 7.3, are utilized [122], [123]. The two Schottky gates are with 2-µm L_G and 180-µm W_G, equally spaced at 5 µm from another ohmic contact. During the measurements, the middle Schottky gate and the ohmic contact are both connected to common ground, whereas the other gate is reversely biased.

Under such bias condition, it can be assured that the current that passes through the ohmic contact equates the reverse gate leakage current (vertical current component, I_V), and the path for the current that flows from the middle Schottky gate to the other one should locate above the AlGaN barrier. Confirmed by the same measurements performed on dual MIS gate structures where minute currents are found to flow from the middle MIS gate to the other one, the main conductive route between the two Schottky gates should therefore be the Al_2O_3/AlGaN interface (interface current, I_{IT}). As shown in Figure 7.3, with PMA, I_V and I_{IT} are reduced by around three and two orders of magnitude, respectively, echoing the reduction of $|I_G|$ and $I_{D,OFF}$ shown in Figure 7.1.

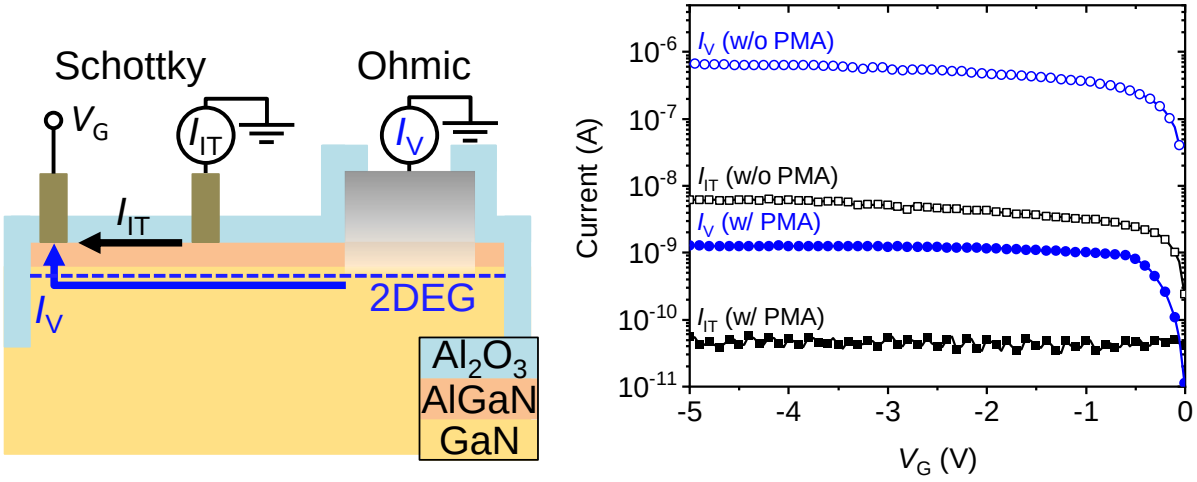

Figure 7.3. Reverse gate leakage current (vertical current component, I_V) and Al_2O_3/AlGaN interface current (I_{IT}) comparisons, with and without PMA.

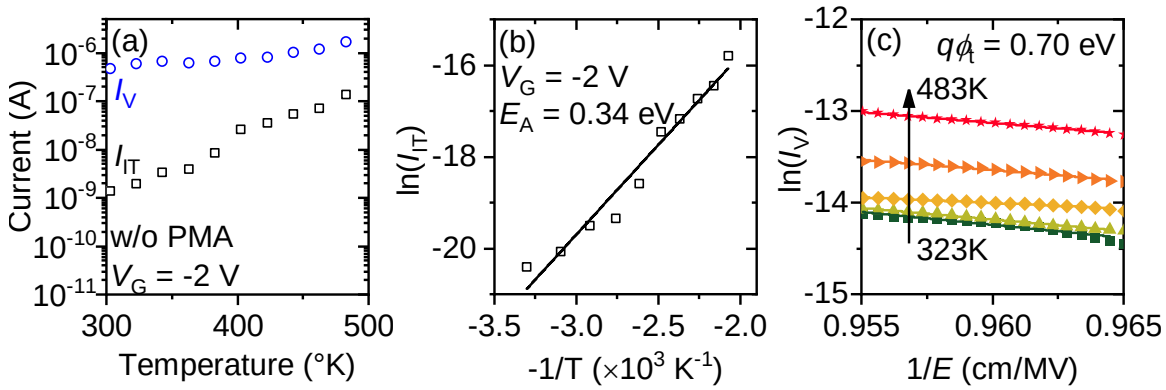

Figure 7.4. (a) Temperature-dependent I-V measurement on the dual Schottky gate structure without PMA. (b) I_{IT} activation energy extraction. (c) AlGaN barrier trap state energy extraction from I_V using TAT model.

In order to study the effect of PMA on the conduction mechanisms of I_{IT} and I_V, temperature-dependent current-voltage (I-V) measurements with the same bias condition are performed on the dual Schottky gate structures, with and without PMA. Without PMA, both I_{IT} and I_V exhibit temperature dependence, as shown in Figure 7.4(a). Utilizing the model of surface/interface conduction due to excitation of electron to conduction band at high temperature regime [124]

$$\sigma_{IT}(T) \propto \exp(-E_A/kT), \tag{7.1}$$

where σ_{IT}, E_A, k, and T are interface conductivity, activation energy, Boltzmann's constant, and temperature (K), respectively, an E_A is extracted as 0.34 eV at V_G = -2 V for I_{IT} (Figure 7.4(b)). This indicates that Al_2O_3/AlGaN interface trap states at 0.34 eV below the conduction band edge are responsible for the high I_{IT} which accounts for a significant portion of $I_{D,OFF}$ that flows from drain directly to gate via the Al_2O_3/AlGaN interface in the Schottky-gate HEMT without PMA. It is worth mentioning that the extracted E_A is close to the value reported in [123]. On the other hand, among several thermionic emission models that are often used to describe temperature-dependent reverse gate leakage current (I_V), the trap-assisted (TA) tunneling model [91]

$$I_V \propto \exp\left[-\frac{8\pi\sqrt{2qm^*}}{3hE}\phi_T^{3/2}\right], \tag{7.2}$$

where E, q, ε, m^*, h, and $q\phi_T$ are electric field across AlGaN barrier, elementary charge, permittivity of AlGaN barrier, electron effective mass in AlGaN barrier, Planck's constant and barrier trap state energy, respectively, best fits the measured I_V (Figure 7.4(c)). The slope of $\ln(I_V)$ versus $1/E$ then yields a trap state energy of 0.70 ± 0.05 eV in the AlGaN barrier.

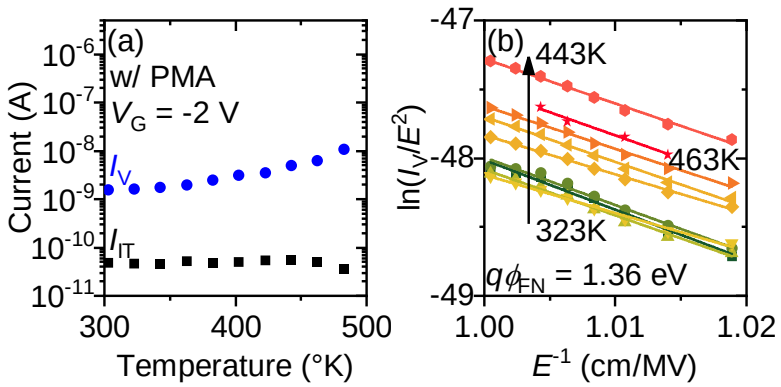

Figure 7.5. (a) Temperature-dependent I-V measurement on the dual Schottky gate structure with PMA. (b) FN tunneling barrier height extraction from I_V.

With PMA, not only do both I_{IT} and I_V decrease by orders of magnitude, but the dominant conduction mechanisms are also altered. As shown in Figure 7.5(a), I_{IT} exhibits no trait of temperature dependence, indicating that the density of Al_2O_3/AlGaN interface trap states at 0.34 eV below the conduction band edge has been greatly reduced by PMA, resulting in a conduction presumably dominated by tunneling. In fact, the increase of $I_{D,on}$ in the HEMT after PMA, as shown in Figure 7.1, is readily another evidence of reduction of density of Al_2O_3/AlGaN interface trap states, since the trapping effect is reduced and thus the 2DEG concentration increases. In addition, it is found that the dominant mechanism of reverse gate leakage also transitions from TA tunneling to Fowler–Nordheim (FN) tunneling [91]

$$I_V \propto E^2 \times \exp\left[-\frac{8}{3}\frac{\pi\sqrt{2m^*}}{qh}\frac{(q\phi_{FN})^{3/2}}{E}\right], \tag{7.3}$$

where E, m^*, h, and $q\phi_{FN}$ are electric field across AlGaN barrier, electron effective mass in AlGaN barrier, Planck's constant, and FN tunneling barrier height, respectively. The slopes of $\ln(I_V/E^2)$ versus E^{-1} (Figure 7.5(b)) yield an average $q\phi_{FN}$ of 1.36 eV, in line with the previously reported value of Ni/$Al_{0.23}Ga_{0.77}N$ Schottky barrier height [125], with a weak temperature dependence.

Capacitance-voltage (C-V) measurements at 100 kHz, 50 mVrms, and 50 mV/s ramp speed are also performed on multiple Ni/Al_2O_3/AlGaN/GaN MIS HEMT capacitors in order to further understand the Al_2O_3/AlGaN interface characteristics. With PMA, an average V_T shift of −1.53 V is observed. We attribute this to the elimination of acceptor-like interface trap states that become negatively charged when occupied. To extract voltage hysteresis (ΔV_T), dual-sweep C-V measurements are also performed (Figure 7.6(a)). During the voltage sweeping, the maximum V_G's are set to 0 V and 1.53 V for the capacitors with and without PMA, respectively, in order to achieve the same maximum overdrive voltage ($V_{GS} - V_T$) for fair comparisons. The extracted ΔV_T's are 33.1 ± 20.2 and 157.0 ± 28.1 mV for the capacitors with and without PMA, which correspond to densities of slow (time constant ≥ ~ 80 s) interface trap states of 6.88×10^{10} and 3.55×10^{11} cm^{-2}, respectively [75]. Results of frequency-dependent C-V measurements are also shown in Figure 7.6(b) and (c). It can be observed that without PMA, the MIS HEMT capacitor exhibits a larger frequency dispersion in the accumulation regime, indicating a higher density of Al_2O_3/AlGaN interface trap states interpreted based on Castagné–Vapaille method [126]. For the MIS HEMT capacitor without PMA, the onset of apparent drop of capacitance takes place at around 200 ~ 500 kHz, corresponding to a trap state energy ($E_C - E_T$) of 0.33 ~ 0.31 eV based on Shockley-Read-Hall statistics

$$\tau_{it} = \frac{1}{2\pi f} = \frac{1}{v_{th}\sigma_{th}N_C}\exp\left(\frac{E_C - E_T}{kT}\right), \tag{7.4}$$

where the average thermal velocity of electron (v_{th}), trap state capture cross section (σ_{th}), and effective density of states in the conduction band (N_C) are 2×10^7 cm/s, 1×10^{-14} cm^2, and $4.3 \times 10^{14} \times T^{3/2}$ cm^{-3}, respectively, for GaN [75]. The identified trap state energy closely matches the extracted E_A (0.34 eV) of the I_{IT} from the dual Schottky gate structure without PMA, confirming that interface trap states at this energy level should be responsible for the Al_2O_3/AlGaN interface

conduction. On the other hand, for the MIS HEMT capacitor with PMA, accumulation capacitance starts to drop at around 1 MHz, corresponding to a trap state energy 0.29 eV. However, the I_{IT} from the dual Schottky gate structure with PMA does not seem to share the apparent temperature dependence, suggesting that the density of interface trap states at this energy level is not high enough to induce the temperature-dependent interface conduction. It is however worth mentioning that the frequency-dependent conductance method is not employed in this work for the extraction of the density of interface trap states, since it has been suggested that the relatively high conductivity of the Al_2O_3/AlGaN interface in the access regions renders the conventionally used equivalent circuit model inaccurate [60].

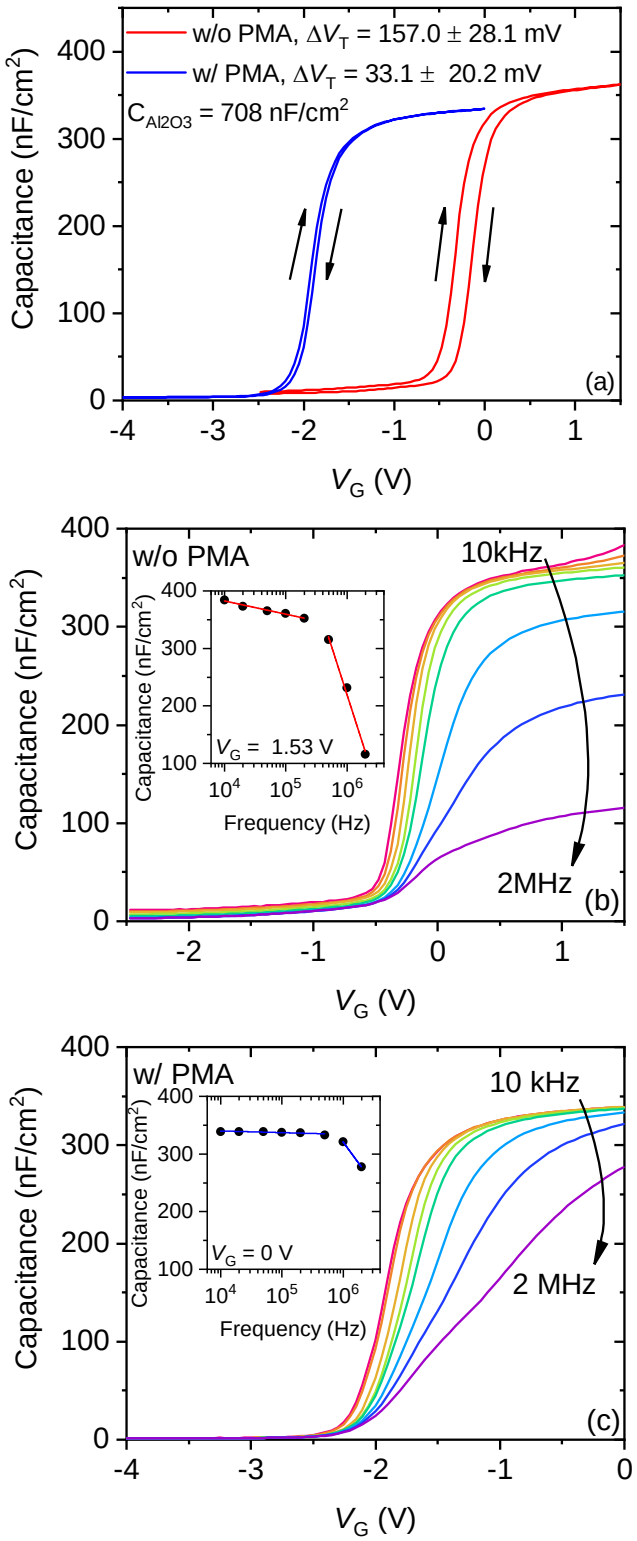

Figure 7.6. Results of (a) dual-sweep C-V measurements and (b) and (c) frequency-dependent C-V measurements. Insets of (b) and (c) show the drop of capacitances at the corresponding maximum voltage as frequency increases.

7.4 Conclusion

In conclusion, effects of PMA on improving the performance of Schottky-gate AlGaN/GaN HEMTs are systematically investigated and cross-compared with different approaches. With PMA, considerable improvements in $I_{D,on/off}$ and *S.S.* of Schottky-gate AlGaN/GaN HEMTs are demonstrated. Confirmed by temperature-dependent I-V measurements on dual Schottky gate structures with Al_2O_3 passivation and C-V measurements on Al_2O_3/AlGaN/GaN MIS HEMT capacitors, we identify that without PMA, Al_2O_3/AlGaN interface trap states with a trap state energy of 0.34 eV are responsible for the Al_2O_3/AlGaN interface leakage current that accounts for a significant amount of $I_{D,off}$. Furthermore, the reverse gate leakage current is found to be dominated by TA tunneling with an AlGaN barrier trap state energy of 0.70 eV. With PMA, Al_2O_3/AlGaN interface leakage current is greatly reduced and exhibits no temperature dependence, indicating an altered conduction mechanism thanks to the elimination of Al_2O_3/AlGaN interface trap states (0.34 eV). Additionally, due to PMA the reverse gate leakage current is also largely reduced, and its dominant mechanism has transitioned to FN tunneling with a barrier height of 1.36 eV. Overall, our work demonstrates improved performance of Schottky-gate AlGaN/GaN HEMTs due to reduced reverse gate leakage current and Al_2O_3/AlGaN interface current by PMA and concludes the corresponding underlying improving mechanisms.

CHAPTER 8 CONCLUSIONS

(Al)GaN-based transistors are the backbones of next generation high power/frequency electronics thanks to the high thermal and chemistry stabilities and the capabilities of handling high-power and high-frequency operations. However, various challenges with such exciting technology still necessitate more comprehensive investigations

We have studied the effect of buffer layer configurations on the 2DEG mobility in AlGaN/GaN HEMT heterostructures on Si(111). Through material, structural, and electrical measurements and analysis, it is shown that a low GaN in-plane tensile strain/stress allows a higher 2DEG mobility due to the alleviated interface roughness scattering. Given similar amount of 2DEG sheet concentration, a distinctively higher 2DEG mobility allows a higher g_m and thus f_T.

In addition, in order to reduce parasitic resistance for further increasing f_T, we have optimized the three-step rapid thermal annealing recipe to achieve a low source/drain metal contact specific resistance (~ 4×10^{-6} Ω–cm^2) using Ti/Al/Ni/Au metal stacks. However, the rough metal surface morphology due to the high-temperature process requires further attention for high-speed device designs. A better approach would be having the source and drain regions readily heavily n-type doped such that the high-temperature annealing process could be avoided.

On the other hand, we have investigated the density of Al_2O_3/(Al)GaN interface trap states in annealed, thin-Al_2O_3/AlGaN/GaN MIS HEMT capacitors fabricated using passivation-first process where the ALD Al_2O_3 is subjected to the high-temperature RTA. Different C-V measurements are used to highlight the density of interface trap states with various time constants, and it is demonstrated that the MIS HEMT capacitor possesses very low $D_{it,slow}$ (extracted from the dual-sweep C-V measurements) but rather high $D_{it,fast}$ (extracted from frequency-dependent

conductance measurements) across the selected range of trap state energy level compared to the results from the literature. In addition, temperature-dependent I-V measurements are performed in order to investigate the dominant leakage mechanism across the annealed thin Al_2O_3 layer. Overall, it is reported that annealed, thin-Al_2O_3 dielectric is an effective (Al)GaN surface passivation alternative for minimizing passivation-associated parasitic capacitance, yet non-ideal for significantly suppressing gate leakage current in MIS structures due to the governing trap-assisted tunneling carrier transport mechanism.

We have also demonstrated the 3.5-μm-Schottky-gate AlGaN/GaN HEMT DC performance where V_T and g_m are extracted as -0.87 V and 131.67 mS/mm, respectively, at V_{DS} = 3.5 V. In addition, $I_D - V_{DS}$ family curves exhibit decent pinch-off behavior with V_{DS} up to 10 V, and $I_{D,ON/OFF}$ and subthreshold swing are extracted as 36kX and 170 mV/dec, respectively. High Schottky gate leakage current and $I_{D,OFF}$ are observed from the $I_D/|I_G| - V_{GS}$ plot, which are believed to be responsible for the large *S.S.* and low $I_{D,ON/OFF}$ ratio.

Since high-temperature-induced degradation of ALD Al_2O_3 has been previously reported, it is presumed to be the root cause of the rather high $D_{it,fast}$ in the MIS HEMT capacitors. In addition, the high Schottky gate leakage current is presumably attributed to the leakage pathways associated with threading dislocations and also thru-mesa-sidewall leakage directly from the Schottky gate to the 2DEG channel. As a result, a new process flow is proposed in which (1) *the ALD Al_2O_3 is deposited after the high-temperature annealing for forming ohmic contacts*, in order to avoid degradation, and (2) *the mesa sidewalls will also be passivated by the ALD Al_2O_3* in order to reduce Schottky gate leakage current. However, it is later discovered that without an annealing after the ALD Al_2O_3 passivation, a large amount of Al_2O_3/AlGaN interface leakage current results in even worse *S.S.* and $I_{D,ON/OFF}$ ratio of the Schottky-gate AlGaN/GaN HEMTs. Therefore, the post-

metallization annealing is employed, and both the reverse biased gate leakage current and off-state drain current are reduced by more than three orders of magnitude, leading to a low subthreshold swing of 84.75 mV/dec and a high drain current on/off ratio of 2.1×10^7.

With the presented studies and conclusions, the next step will be adapting these results and optimized process flows for fabrication of AlGaN/GaN HEMTs with sub-100-nm gate length in T-gate configuration using electron beam lithography. In addition, proper layout designs considering RF transmission line effects and high-frequency device parameter de-embeddings are to be implemented. Ultimately, continued studies following this dissertation are to fuel the development of AlGaN/GaN HEMTs towards reliable high-speed electronics for 5G telecommunication technology and beyond.

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APPENDIX A TRANSMISSION LINE MEASUREMENT ANALYSIS METHOD

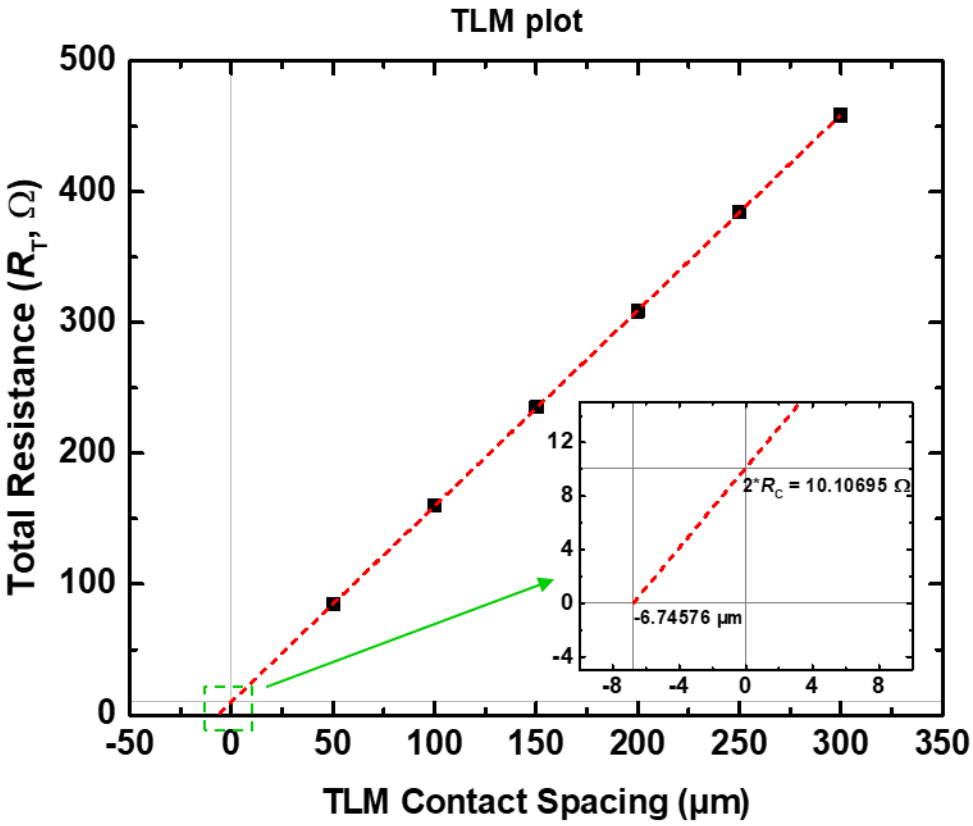


Figure A.1. TLM data fitting.

$R_C = \frac{10.10}{2} = 5.05\ \Omega$

$R_S = \text{slope} \times W = 1.49(V/\mu\text{m}) \times 200\mu\text{m} = 298\ \Omega/\square$

$R_{Tol} = 2R_C + (R_S/W)(-2L_T)$, L_T is the transfer length;

$0 = 10.10 + 1.49 \times (-2L_T)$;

$L_T = 3.389\mu\text{m}$

$\rho_C = R_C \times L_T \times W = 5.05\ \Omega \times 3.389 \times 10^{-4}\text{cm} \times 200 \times 10^{-4}\text{cm}$;

$\rho_C = 3.423 \times 10^{-5}\Omega \cdot \text{cm}^2$, ρ_C is the specific resistance;

$R_T = R_C \times W = 5.05\ \Omega \times 0.2\text{mm} = 1.01\ \Omega \cdot \text{mm}$, R_T is the contact resistance.

APPENDIX B DESIGNS OF PHOTOMASK AND PASSIVATION-FIRST PROCESS

The designed photomask has a die size of 5671 μm × 5922 μm, and the smallest feature size is 1 μm. In each die there are 12 × MIS capacitors (2 repeats), 12 × Schottky capacitors (2 repeats), 30 × AlGaN/GaN HEMTs (with 180-μm gate width), 30 × AlGaN/GaN HEMTs (with 90-μm gate width), 3 sets of TLM patterns for (i) S/D (ohmic) metal contacts, (ii) Schottky gate metal contacts, and (iii) MIS gate metal contacts, process control marks: (i) 6 sets for lithography and (ii) 4 sets for etching, 9 sets of alignment marks (aligning to the passivation opening mask), and 5 sets of alignment marks (aligning to the mesa isolation mask), as shown below. The photomask design contains 6 sub-masks; their functionalities are: mask #1 passivation opening; mask #2 S/D metal deposition; mask #3 gate opening; mask #4 gate metal deposition; mask #5 mesa isolation; and mask #6 contact window opening. Mask #5 mesa isolation can also be used as the first layer of mask; the alignment marks are designed accordingly.

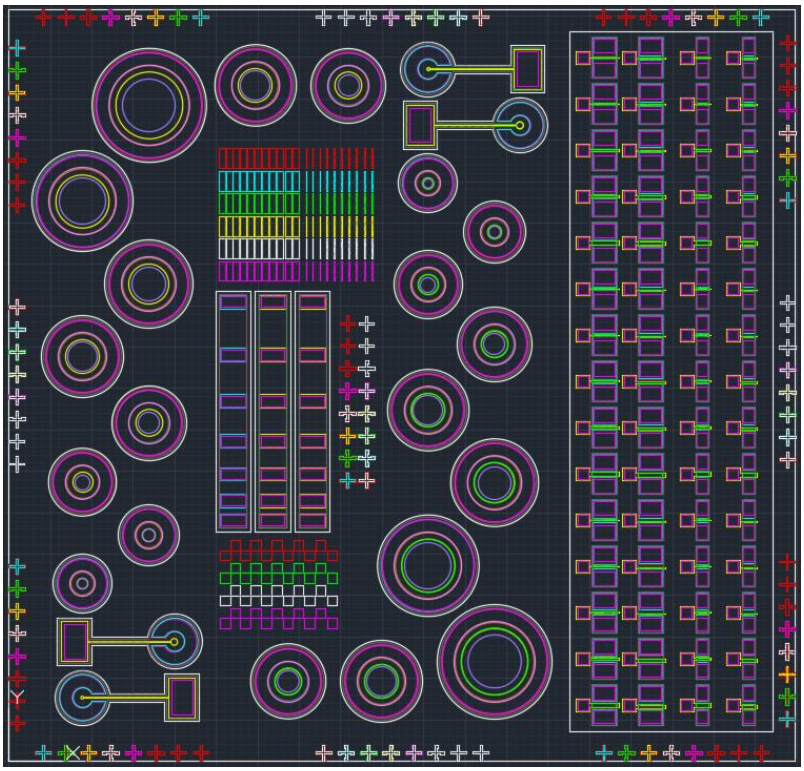


Figure B.1. Design of photomask of passivation-first process.

B.1 Device dimensions

Table B.1. MIS Capacitors (with dielectric layer between gate metal contact (inner contact) and GaN).

Device #	Inner contact diameter (μm)	Distance between electrodes (μm)	Outer electrode opening (μm)	Wire width (μm)
D101	500	50	No opening	No wire
D102	400	50	No opening	No wire
D103	300	50	No opening	No wire
D104-1 D104-2	250	50	No opening	No wire
D105-1 D105-2	200	50	No opening	No wire
D106	150	50	No opening	No wire
D107	100	50	No opening	No wire
D108	80	50	No opening	No wire
D109	50	50	60	5
D110	20	75	60	5

Table B.2. Schottky Capacitors (without dielectric layer between gate metal contact (inner contact) and GaN).

Device #	Inner contact diameter (μm)	Distance between electrodes (μm)	Outer electrode opening (μm)	Wire width (μm)
D201	500	50	No opening	No wire
D202	400	50	No opening	No wire
D203	300	50	No opening	No wire
D204-1 D204-2	250	50	No opening	No wire
D205-1 D205-2	200	50	No opening	No wire
D206	150	50	No opening	No wire
D207	100	50	No opening	No wire
D208	80	50	No opening	No wire
D209	50	50	60	5
D210	20	75	60	5

Table B.3. AlGaN/GaN HEMTs (symmetric) (containing both 180- and 90-µm gate widths).

Device #	Gate length (µm)	Gate width (µm)	L_{GS} (µm)	L_{GD} (µm)
T101 / T301	2	180 / 90	5	5
T102 / T302	5	180 / 90	5	5
T103 / T303	10	180 / 90	5	5
T104 / T304	20	180 / 90	5	5
T105 / T305	30	180 / 90	5	5
T106 / T306	2	180 / 90	10	10
T107 / T307	5	180 / 90	10	10
T108 / T308	10	180 / 90	10	10
T109 / T309	20	180 / 90	10	10
T110 / T310	30	180 / 90	10	10
T111 / T311	2	180 / 90	15	15
T112 / T312	5	180 / 90	15	15
T113 / T313	10	180 / 90	15	15
T114 / T314	20	180 / 90	15	15
T115 / T315	30	180 / 90	15	15

Table B.4. AlGaN/GaN HEMTs (asymmetric) (containing both 180- and 90-µm gate widths).

Device #	Gate length (µm)	Gate width (µm)	L_{GS} (µm)	L_{GD} (µm)
T201 / T401	2	180 / 90	10	20
T202 / T402	5	180 / 90	10	20
T203 / T403	10	180 / 90	10	20
T204 / T404	20	180 / 90	10	20
T205 / T405	30	180 / 90	10	20
T206 / T406	2	180 / 90	5	25
T207 / T407	5	180 / 90	5	25
T208 / T408	10	180 / 90	5	25
T209 / T409	20	180 / 90	5	25
T210 / T410	30	180 / 90	5	25
T211 / T411	2	180 / 90	5	30
T212 / T412	5	180 / 90	5	30
T213 / T413	10	180 / 90	5	30
T214 / T414	20	180 / 90	5	30
T215 / T415	30	180 / 90	5	30

B.2 Additional mask designs

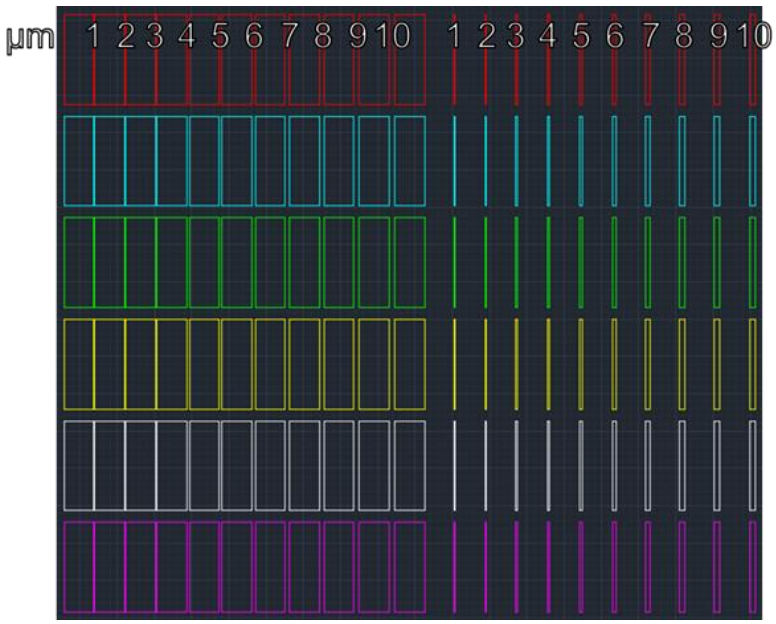


Figure B.2. Over/under-development investigation marks.

To check the over-etching, if any two adjacent squares contact with each other, then the "over-etching" is quantified as half of the original distance, which is shown as the numbers labeled.

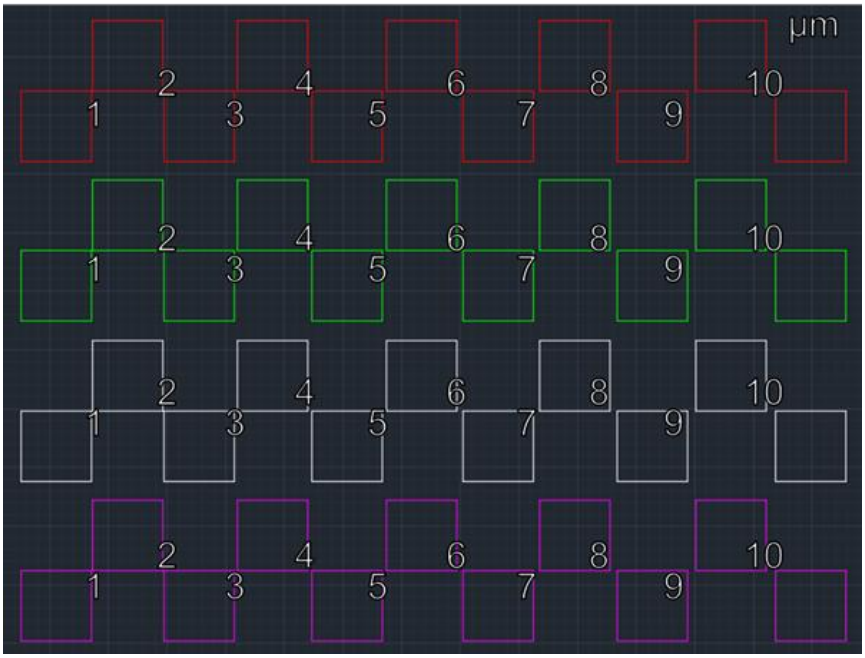


Figure B.3. Over-etching investigation marks.

The measured resistance between two adjacent pads is equal to $2R_{pad} + R_{semi}$. The spacings between these pads are 50, 100, 150, 200, 250, 300 μm; the measured resistances will form a straight line in a resistance-position plot, where the intersection of the y-axis represents the value of $2R_{pad}$, hence R_{pad} is obtained. Using R_{pad} to multiply with the pad surface area (100 μm × 200 μm), contact resistance (Ω–cm^2) is therefore obtained.

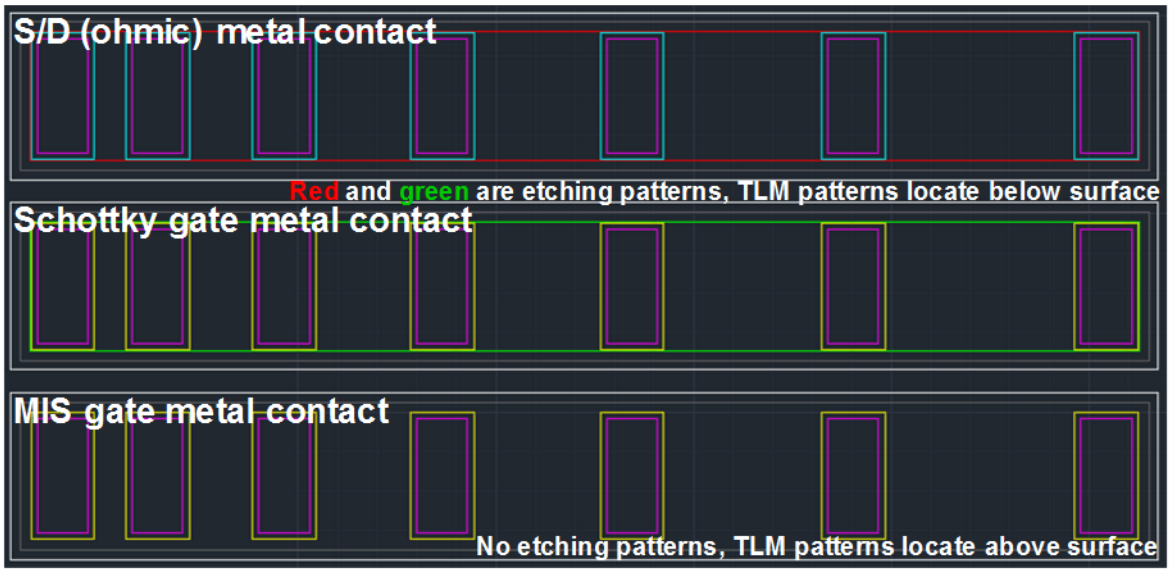


Figure B.4. TLM patterns.

Nine sets of alignment marks for aligning to Mask #1 (red, dark field): Mask #2 (blue, light field); Mask #3 (green, dark field); Mask #4 (yellow, light field); Mask #5 (white, light field); Mask #6 (purple, dark field). Five sets of alignment marks for aligning to Mask #5 (white, dark field): Mask #1 (red, light field); Mask #2 (blue, light field); Mask #3 (green, dark field); Mask #4 (yellow, light field); Mask #6 (purple, dark field)

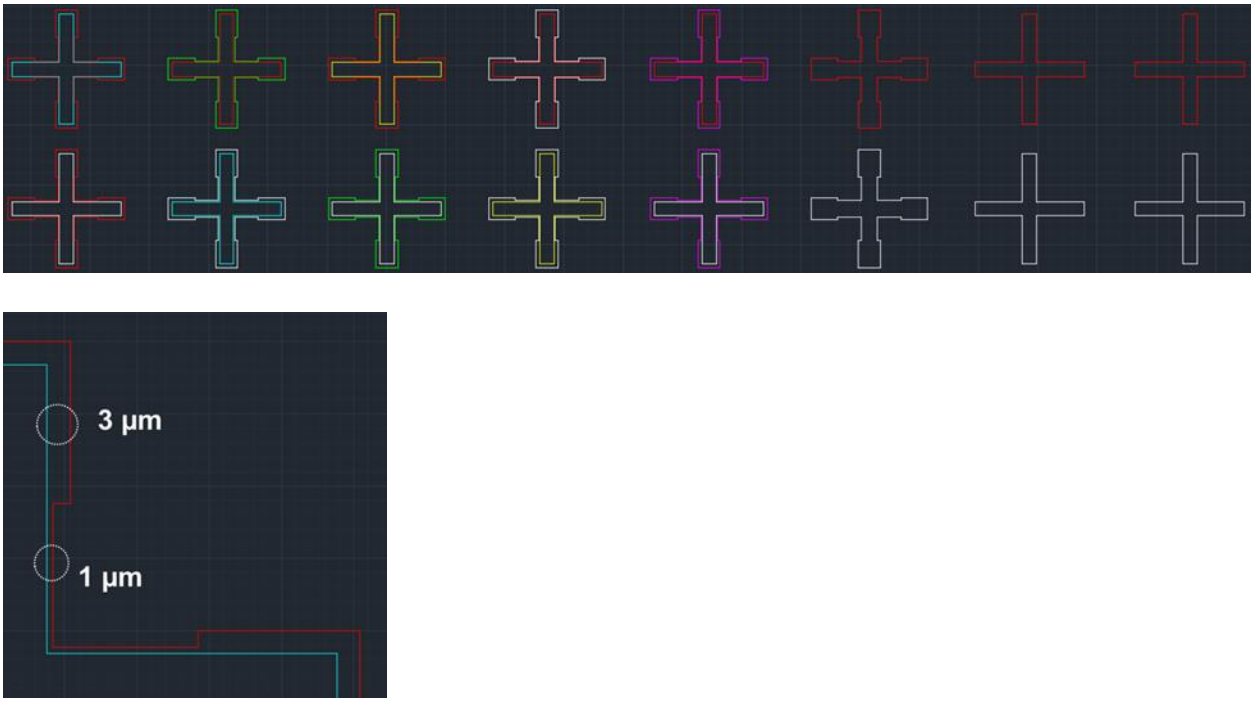


Figure B.5. Alignment marks.

B.3 Fabrication process

For protecting the AlGaN/GaN HEMT surface, Al_2O_3 is first ALD-deposited as a pre-passivation layer. Afterwards positive photolithography (mask #5) is conducted followed by BOE wet etching and chlorine-based ICPRIE for mesa isolation to isolate the capacitors, HEMTs and the TLM patterns. After this, positive photolithography (mask #1) is conducted followed by BOE wet etching for passivation opening. The opened area will then be deposited with Ti/Al/Ni/Au metal stack defined by mask #2 as S/D contacts and then annealed to form ohmic contact. For the HEMTs and the Schottky capacitors, the gate areas (defined by mask #3) will be opened again by BOE wet etching and then deposited with Ni/Au (defined by mask #4) as gate metal contact. Note that the gate metal contacts of MIS capacitors are also formed at this stage. Finally, mask #6 is used for contact window opening after the SiN_x post passivation.

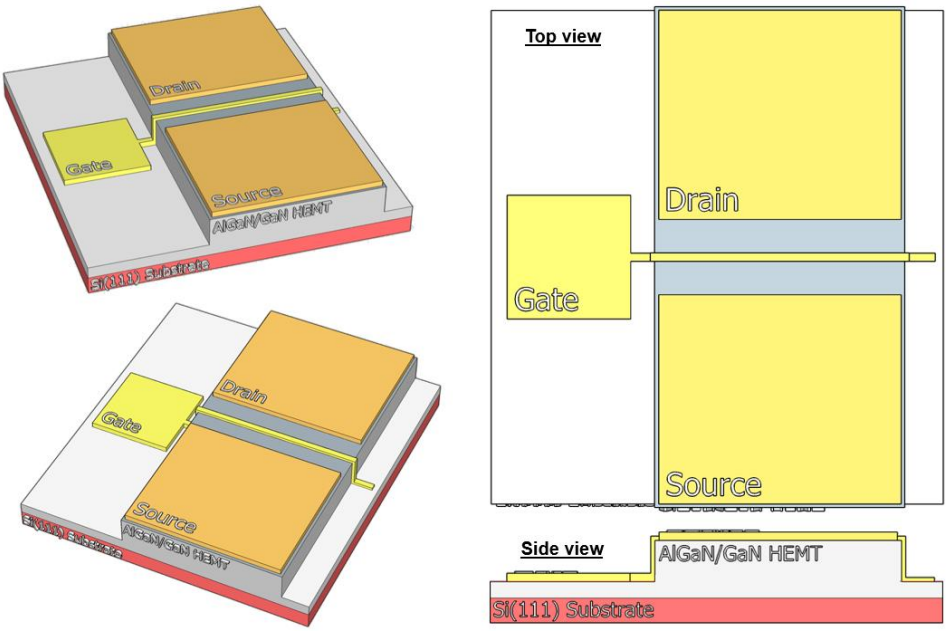


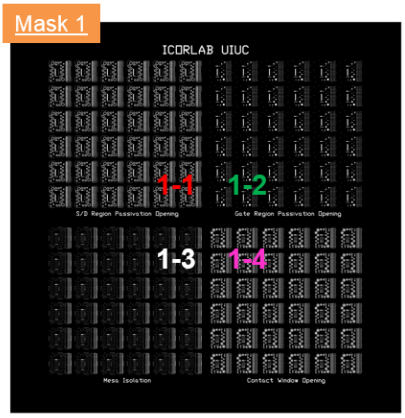
Figure B.6. 3-D schematic AlGaN/GaN HEMT structure on Si(111) substrates.

APPENDIX C DETAILED PASSIVATION-FIRST PROCESS FLOW

*When looking at the mask as shown, the chrome is on the backside.
*Dark region is covered with chrome; white area is transparent.
*Clear: data clear; dark: data dark

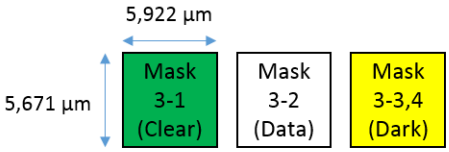
Masks	Quadrant label
Mask 1-1	S/D Region Passivation Opening
Mask 1-2	Gate Region Opening
Mask 1-3	Mesa Isolation
Mask 1-4	Contact Window Opening
Mask 2-1,3	S/D Metal Deposition
Mask 2-2,4	Gate Metal Deposition

Mask 1



Mask 2

*When looking at the mask as shown, the chrome is on the backside.
*Dark region is covered with chrome; white area is transparent.
*Clear: data clear; dark: data dark



Masks	Quadrant label
Mask 3-1	Gate Region Passivation Opening (v2)
Mask 3-2	Mesa Isolation (v2)
Mask 3-3,4	Gate Metal Deposition (v2)

Mask 3

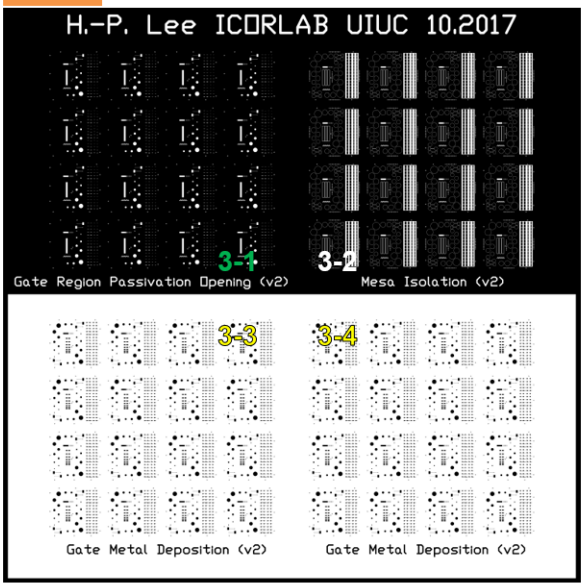


Figure C.1. Illustration of the mask set.

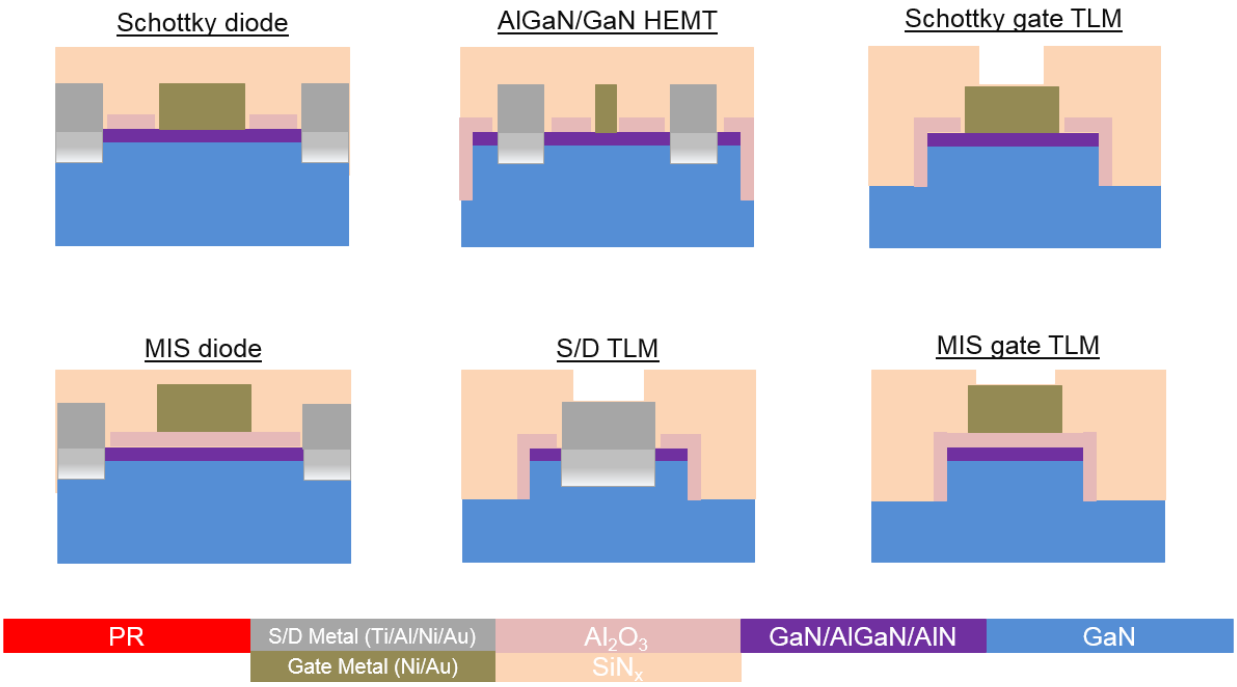


Figure C.2. Illustration of finished device cross section.

Schottky diode and MIS diode

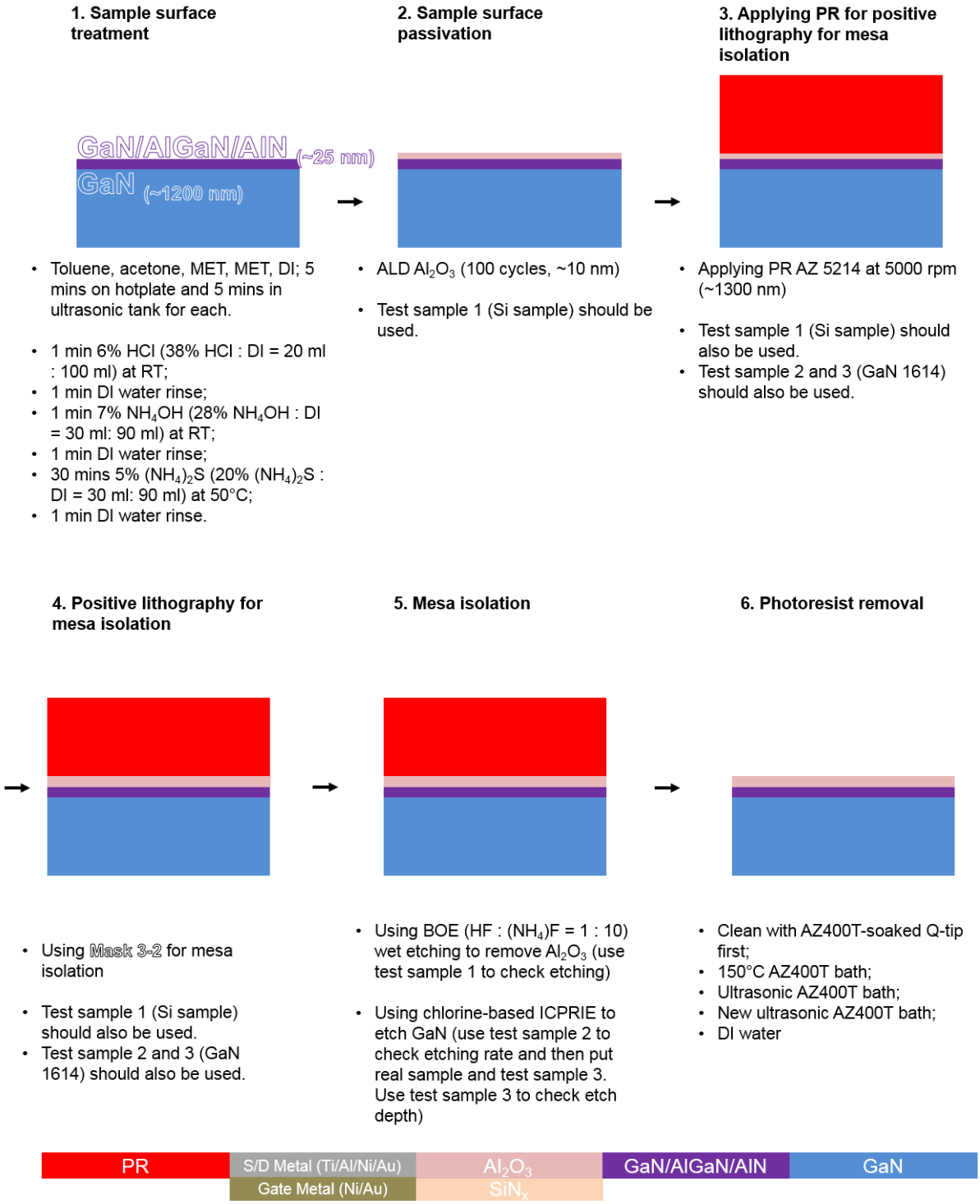


Figure C.3. Illustration of process flow (taking diodes for example, all devices are finished simultaneously).

Schottky diode and MIS diode

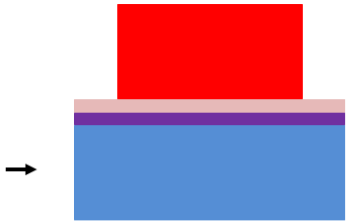
7. Mesa sidewall passivation

- ALD Al_2O_3 (100 cycles, ~10 nm)
- Test sample (Si sample) should be used.

8. Applying PR for positive lithography for S/D region opening

- Applying PR AZ 5214 at 5000 rpm (~1300 nm)
- Test sample 1 (Si sample) should also be used.

9. Positive lithography for S/D region opening



- Using **Mask 1-1** for S/D region passivation opening
- Test sample 1 (Si sample) should also be used.

10. S/D region opening

- Using BOE wet etching to remove Al_2O_3 on the S/D region
- BOE (HF : $(NH_4)F$ = 1 : 10)
- Test sample 1 (Si sample) should also be used.

11. Photoresist removal

- Clean with AZ400T-soaked Q-tip first;
- 150°C AZ400T bath;
- Ultrasonic AZ400T bath;
- New ultrasonic AZ400T bath;
- DI water

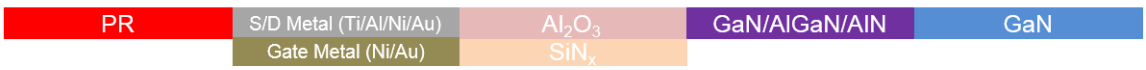


Figure C.3 (continued). Illustration of process flow (taking diodes for example, all devices are finished simultaneously).

Schottky diode and MIS diode

12. Applying PR for negative lithography for S/D metallization

- Applying PR AZ 5214 at 5000 rpm (~1300 nm)
- Test sample 1 (Si sample) should also be used.

13. Negative lithography for S/D metallization

- Using **Mask 2-1 or 2-3** for S/D metallization
- The PR should have negative sidewall angle
- Test sample 1 (Si sample) should also be used.

14. S/D Metallization

- Surface treatment HCl : DI (1:1) at 150°C for 60”
- E-beam evaporator: Ti (20 nm) / Al (120 nm) / Ni (55 nm) / Au (45 nm) (*J. Phys. D: Appl. Phys.* **45**, 265101 (2012))
- Test sample 1 (Si sample) should also be used.

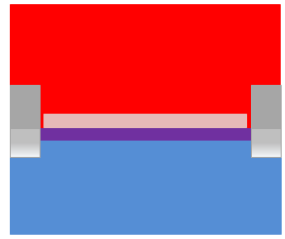
15. Lift-off

- ACE spray, 150°C AZ400T bath for 5 min, DI water bath for 10 min

16. Rapid thermal annealing (for forming ohmic contact)

- Rapid thermal annealing at 870°C for 50 sec (*J. Phys. D: Appl. Phys.* **45**, 265101 (2012))

17. Applying PR for positive lithography for gate region opening



- Applying PR AZ 5214 at 5000 rpm (~1300 nm)
- Test sample 1 (Si sample) should also be used.

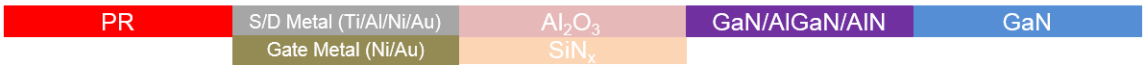


Figure C.3 (continued). Illustration of process flow (taking diodes for example, all devices are finished simultaneously).

Schottky diode and MIS diode

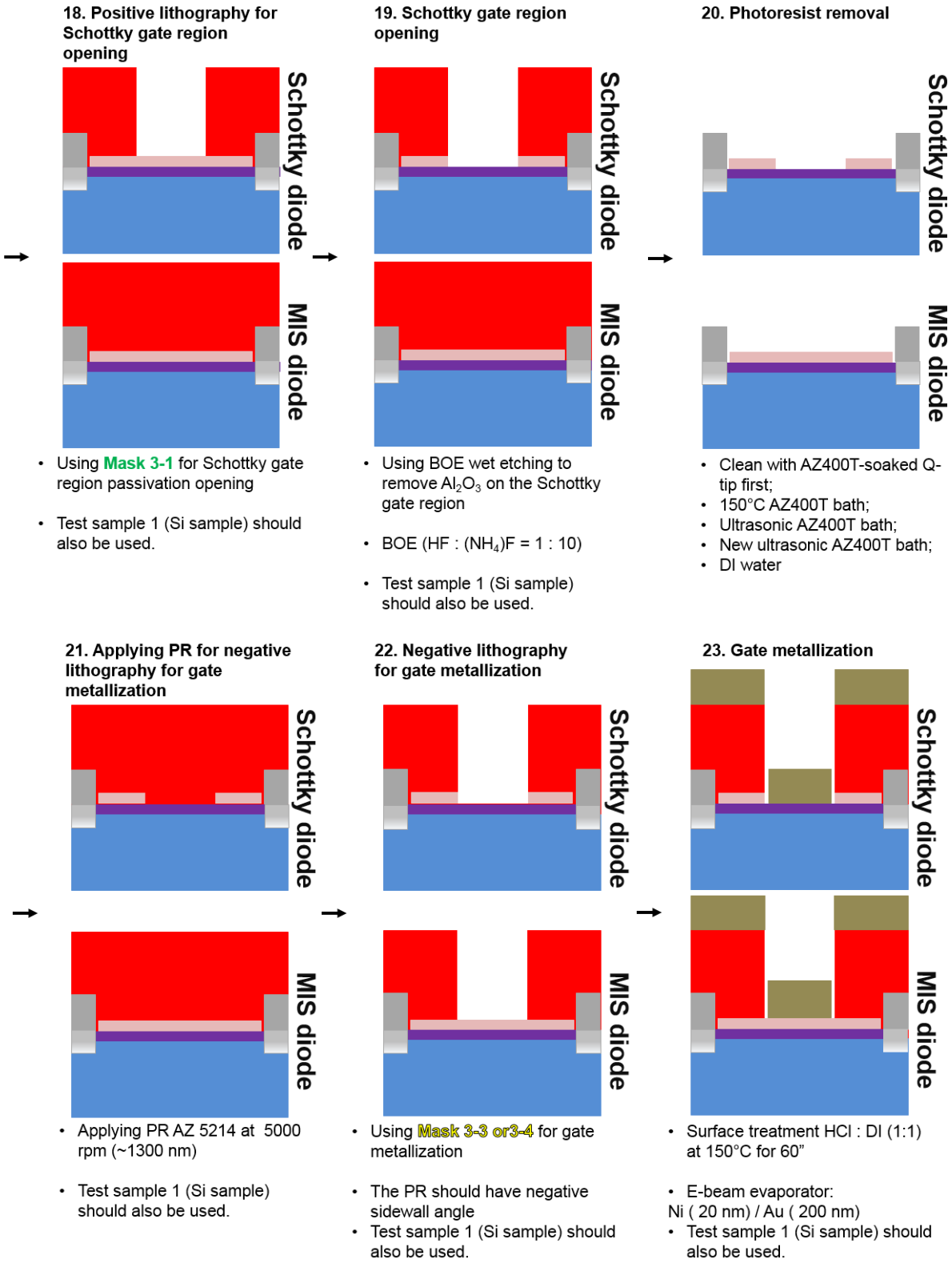


Figure C.3 (continued). Illustration of process flow (taking diodes for example, all devices are finished simultaneously).

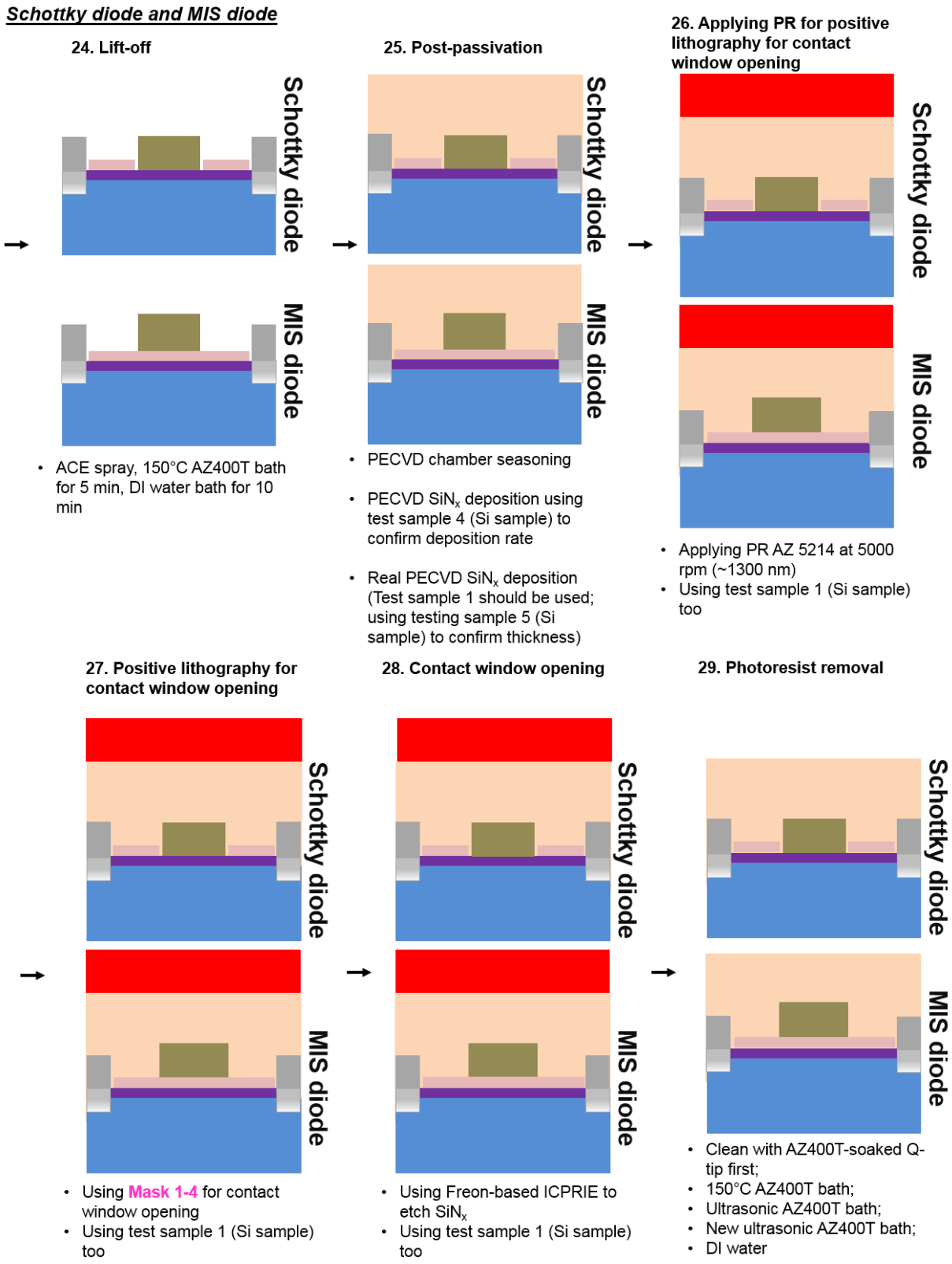


Figure C.3 (continued). Illustration of process flow (taking diodes for example, all devices are finished simultaneously).

APPENDIX D DESIGNS OF PHOTOMASK AND PASSIVATION-LAST PROCESS

- Die size: 0.8×0.8 mm^2
- Capacitors: Schottky and MIS (150 and 300 μm)
- HEMTs:
  - DC: Schottky and MIS (symmetrical and asymmetrical)
  - RF: Schottky and MIS (symmetrical) (GSG probing)
- Testing structures:
  - TLM for ohmic, Schottky, and MIS contacts
  - Van der Pauw w/ and w/o Al_2O_3 passivation
  - Ungated HEMTs w/ and w/o Al_2O_3 passivation
  - Gate-gate-ohmic structure w/ and w/o Al_2O_3 passivation
  - Fat HEMTs: Schottky and MIS (for thermal study with Kihoon)
  - GSG metal pads for RF de-embedding
- Processing marks:
  - Alignment marks for Karl Suss Aligner (cross and Vernier caliper marks (0.2 μm resolution))
  - Alignment marks for Heidelberg direct write system
  - Development marks
  - Etching marks

D.1 Device dimensions

Table D.1. Detailed device/structure information.

Devices	Remarks
MIS capacitors	Diameter: 300 and 150 µm
Schottky capacitors	Diameter: 300 and 150 µm
MIS HEMTs	Symmetric and asymmetric
Schottky HEMTs	Symmetric and asymmetric
MIS and Schottky HEMT	Compatible with GSG probing
Open de-embedding 1 & 2	-/-
Short de-embedding 1 & 2	-/-
Pad de-embedding	-/-
TLM	100 x 200 µm^2
Van der Pauw	w/ and w/o passivation
Gate-gate-ohmic structure	w/ and w/o passivation
Fat-HEMTs	MIS and Schottky
Ungated HEMTs	w/ and w/o passivation

Table D.2. Dimensions of AlGaN/GaN HEMTs.

Symmetric HEMT		Asymmetric HEMT		
L_G (μm)	L_{GS} (L_{GD}) (μm)	L_G (μm)	L_{GS} (μm)	L_{GD} (μm)
2	5	2	5	10
2	10	2	5	15
2	15	2	5	20
5	5	5	5	10
5	10	5	5	15
5	15	5	5	20
10	5	10	5	10
10	10	10	5	15
10	15	10	5	20

Table D.3. Dimensions of gate-gate-ohmic structures.

Gate-gate-ohmic structure		
L_G (μm)	L_{GS} (μm)	L_{GD} (μm)
2	5	5
5	5	5
10	5	5
2	10	10
5	10	10
10	10	10
2	15	15
5	15	15
10	15	15

Table D.4. Dimensions of Fat-HEMTs.

Fat-HEMTs		
L_G (μm)	L_{GS} (μm)	L_{GD} (μm)
10	2	80
50	2	40

Table D.5. Dimensions of ungated HEMTs.

Ungated HEMTs
L_{DS} (μm)
10
20
30
13
23
33
18
28
38

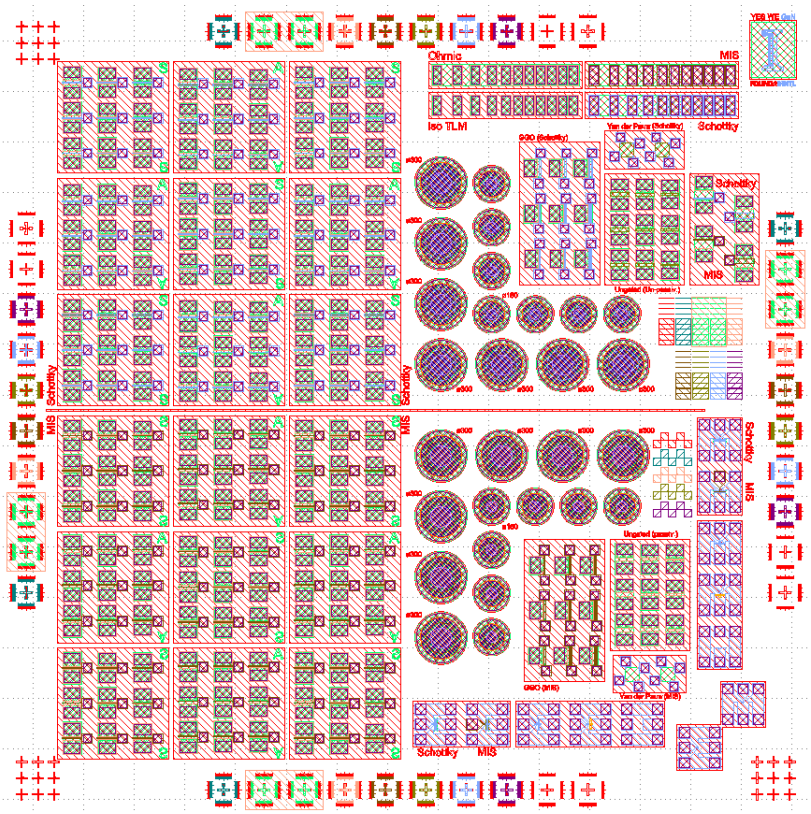


Figure D.1. Design of photomask of passivation-last process.

D.2 Photomask checking

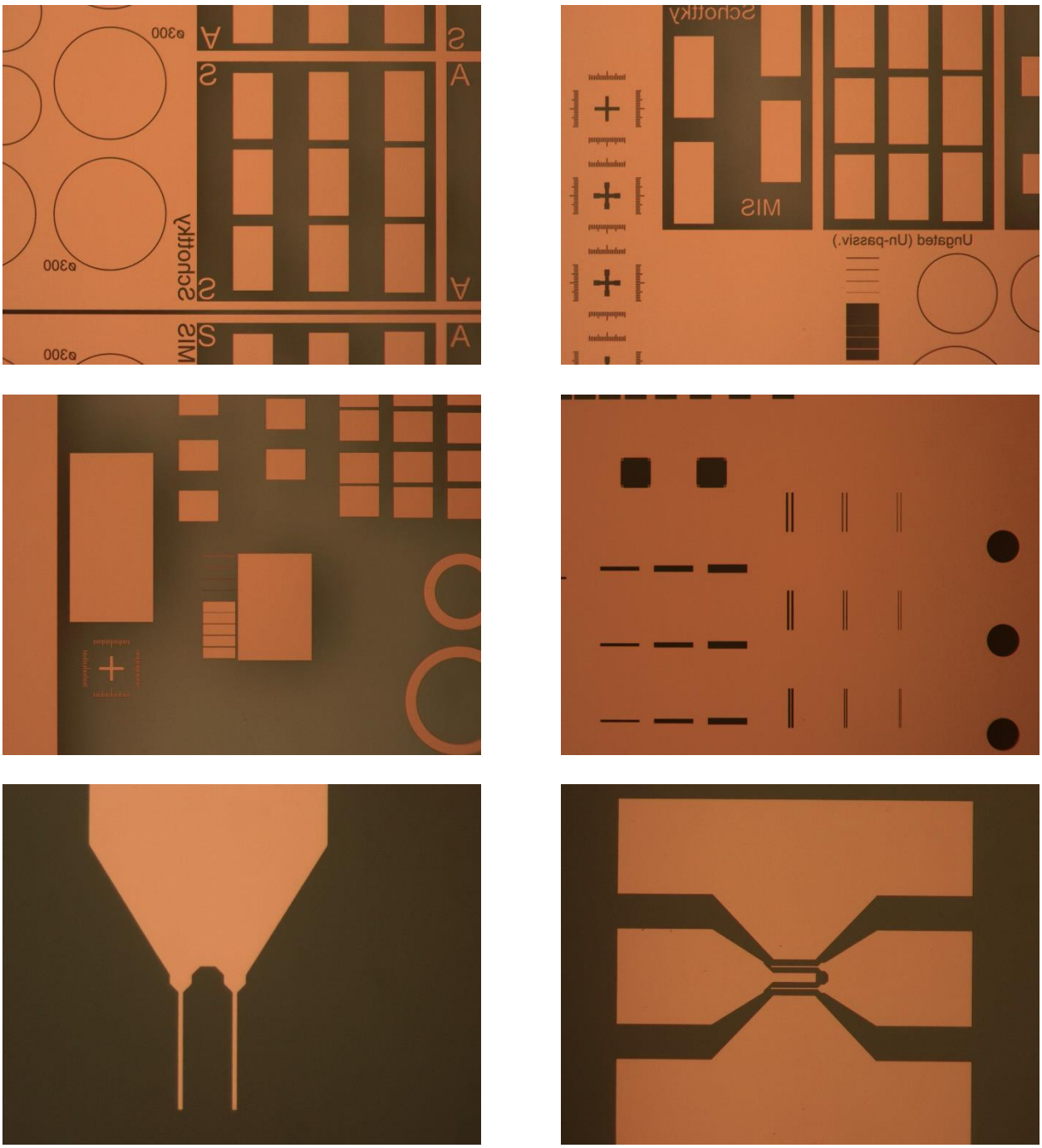


Figure D.2. Optical microscopy images of the photomasks.

APPENDIX E DETAILED PASSIVATION-LAST PROCESS FLOW

Table E.1. Passivation-last process flow.

Step #	Mask #	Purpose	Equipment	Remark
1		GaN surface cleaning and treatment		Toluene, acetone, MET, MET, DI; HCl, NH_4OH, $(NH_2)_4S$, DI
2		1st ALD Al_2O_3 passivation	ALD	10 nm
3	1 (+)	Mesa isolation	ICPRIE	BOE and ICPRIE
4	2 (+)	Ohmic contact opening		BOE
5	3 (-)	Ohmic contact deposition	Ebeam evap. (MRL)	Ti/Al/Ni/Au
6		Rapid thermal annealing	RTA	$T°_{max}$: 900°C
7	4 (-)	Au deposition	Ebeam evap. (MNTL)	10 nm; protect all ohmic contacts from BOE in contact opening (Step 16)
8		2nd ALD Al_2O_3 passivation	ALD	15 ~ 20 nm; protect ohmic contacts from HCl, NH_4OH and $(NH_2)_4S$
9	5 (+)	GaN surface opening		BOE
10		GaN surface treatment		HCl, NH_4OH, $(NH_2)_4S$
11		3rd ALD Al_2O_3 passivation	ALD	10 nm; annealing-free Al_2O_3 on cleaned GaN surface
12	6 (-)	MIS gate deposition	Ebeam evap. (MNTL)	Ni/Au
13	7 (+)	Schottky gate opening		BOE; also open the ohmic contact in GSG HEMTs
14	8 (-)	Schottky gate deposition	Ebeam evap. (MNTL)	Ni/Au; also, on the ohmic contact in GSG HEMTs
15		SiN overall passivation (optional)	PECVD	
16	9 (+)	Contact opening		BOE; open ohmic contacts or all contacts if with SiN passivation

Figure E.1. Illustration of process flow (taking diodes for example, all devices are finished simultaneously).

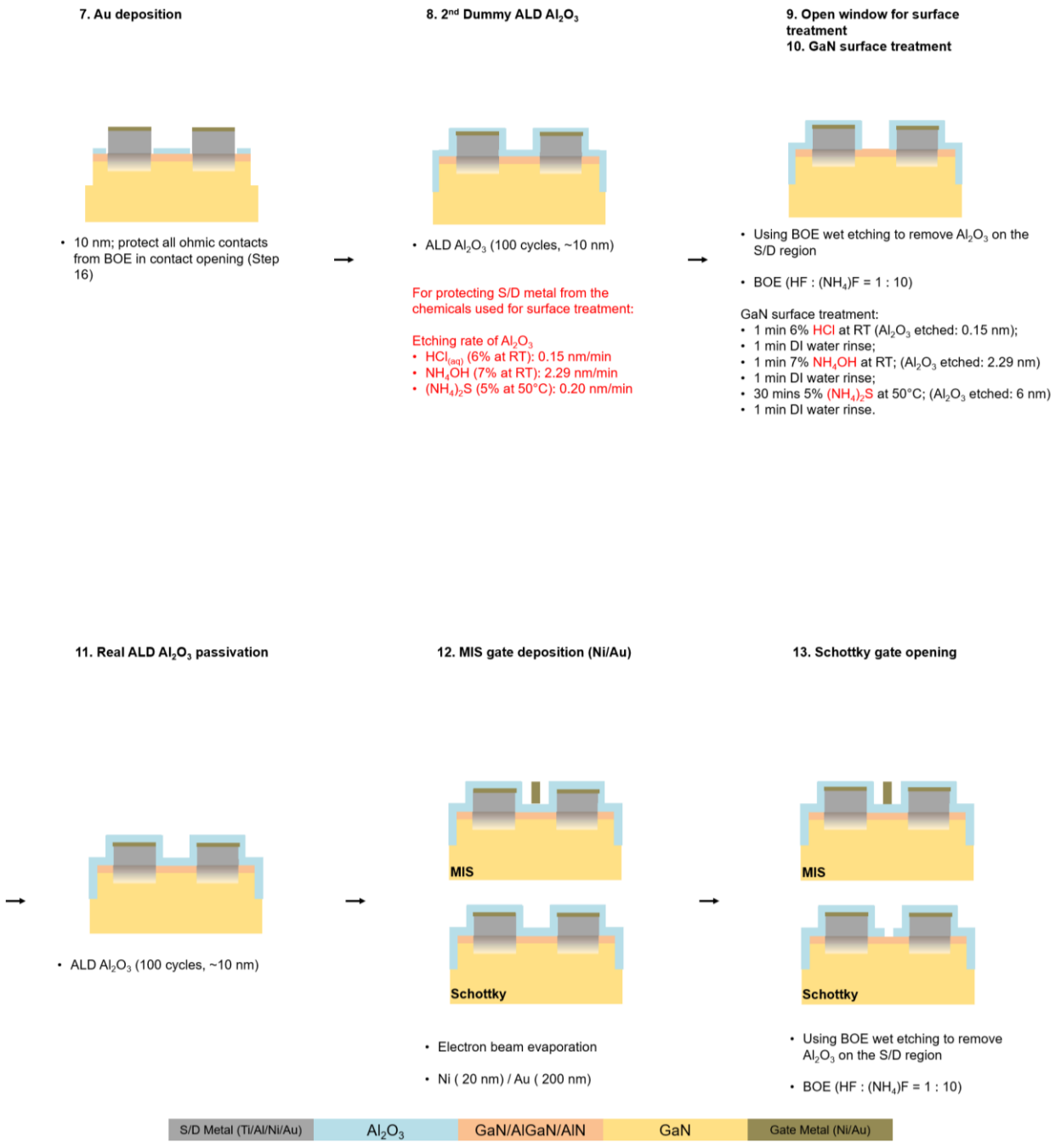


Figure E.1 (continued). Illustration of process flow (taking diodes for example, all devices are finished simultaneously).

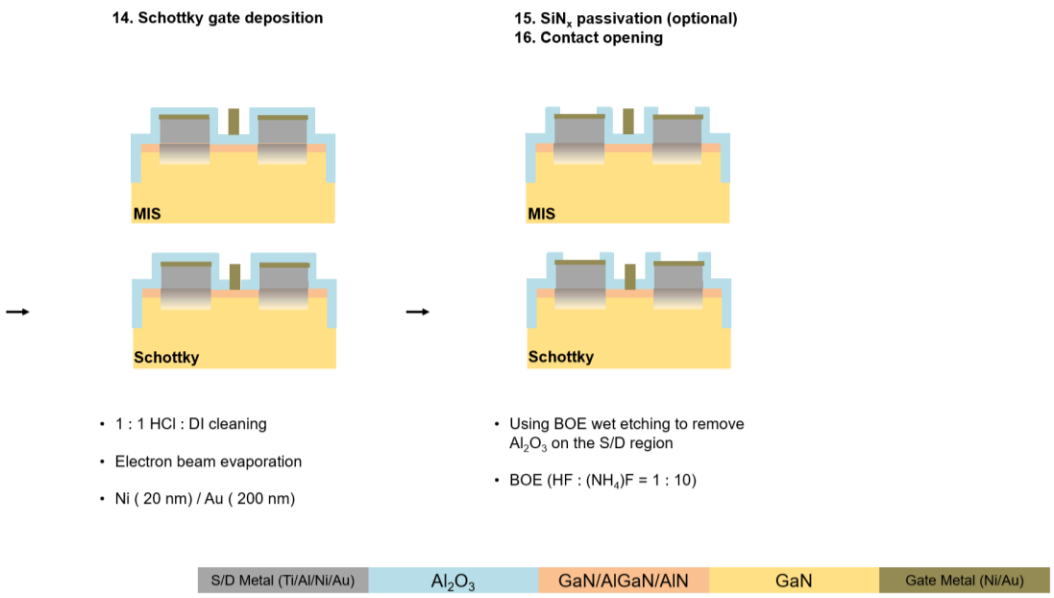


Figure E.1 (continued). Illustration of process flow (taking diodes for example, all devices are finished simultaneously).

E.1 Additional notes

a. AZ 400T is necessary for thoroughly removing the photoresist residue.

AZ400T is a chemical solution that contains N-methyl-2-pyrrolidone (NMP) and 2~5% tetramethylammonium hydroxide (TMAH) and can properly remove the AZ5214 photoresist residue. However, it has been reported that 8% TMAH etches Al_2O_3 in a fairly rapid speed at elevated temperatures by Oh *et al.* (*J. Electrochem. Soc.*, vol. 158, no. 4, pp. 217–222, 2011.), which suggests that AZ400T will likely be incompatible to our newly proposed process method. Therefore, we re-evaluate the effect of using heated AZ400T on the ALD Al_2O_3 via the experiment outlined as follows:

1. 300 cycles of ALD Al_2O_3 (about 30 nm) on BOE'd 2" Si(111)
2. AZ400T temperature: ~ 60°C (set hotplate to 150°C and wait for 10 min)
3. Soaking time: 5 min, 10 min, 15 min, 20 min, 25 min, and 30 min

The results show less than 1 nm reduction in thickness after 30 min (confirmed by ellipsometry and XRR), which contradict the results reported by Oh *et al.* (*J. Electrochem. Soc.*, vol. 158, no. 4, pp. 217–222, 2011.). Therefore, AZ400T will be employed for properly removing the photoresist residue in the future batch of fabrication.

b. The second GaN surface treatment using 6% HCl, 7% NH_4OH, and then 5% $(NH_4)_2S$ is necessary for having decent ALD Al_2O_3/GaN interface quality.

In the new processing method, the real Al_2O_3 passivation is ALD-grown after forming the S/D ohmic contact (Ti/Al/Ni/Au). Prior to the ALD growth, the surface treatment method that was used in the beginning cannot be again used without a proper S/D metal protection due to the incompatibility between the chemicals (HCl, NH_4OH, and $(NH_4)_2S$) and the S/D metal. Without

the surface treatment immediately prior to the real ALD Al_2O_3, from a dual-sweep C-V measurement (Figure E.2), huge hysteresis can be observed from both capacitors, especially in the MIS HEMT capacitor. This indicates higher density of slow interface trap states in the MIS HEMT capacitor are negatively charged during the up-sweep and then remain charged after surfacing above the Fermi level during the down-sweep. Such hysteresis leads to device operation instability and reduces the reliability.

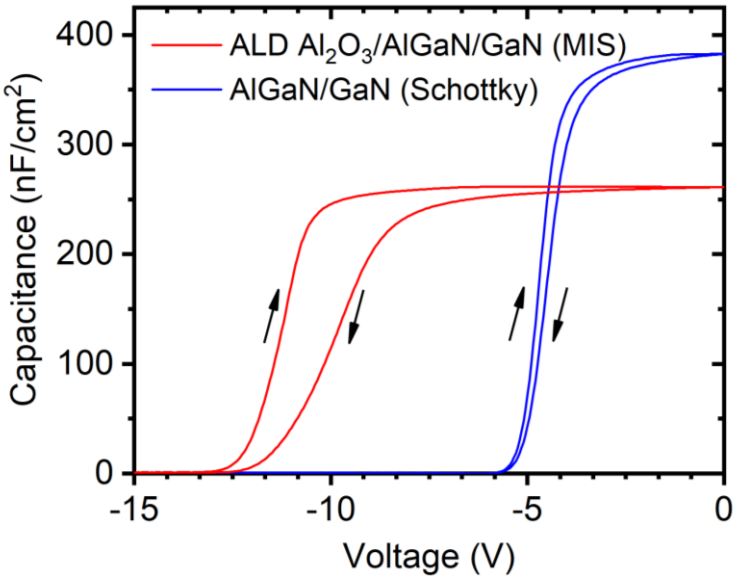


Figure E.2. Dual-sweep capacitance-voltage curves with large voltage hysteresis.

Al_2O_3 is resistive to NH_4OH, and it will be only slowly etched by 1 : 1 HCl : DI water (~ 3 nm/min). However, not much information about the compatibility between Al_2O_3 and $(NH_4)_2S$ can be found in the literature. Once confirmed compatible, we are to use a 2nd dummy 10-nm ALD Al_2O_3 to protect the S/D metal, as mentioned previously, and the GaN surface can then be again conditioned by the chemicals used for surface treatment to improve the Al_2O_3/GaN interface quality.

c. Separation of MIS and Schottky gate deposition.

Separation of MIS and Schottky gate deposition allows different treatment method to be used prior to the metal deposition. For depositing gate metal on Al_2O_3 (MIS gate), simple degrease is generally enough. However, for gate metal deposition on GaN (Schottky gate), hot HCl bath is needed for removing the native oxide. Because hot $HCl_{(aq)}$ (60°C) etches Al_2O_3, separating the MIS and Schottky gate depositions is necessary.

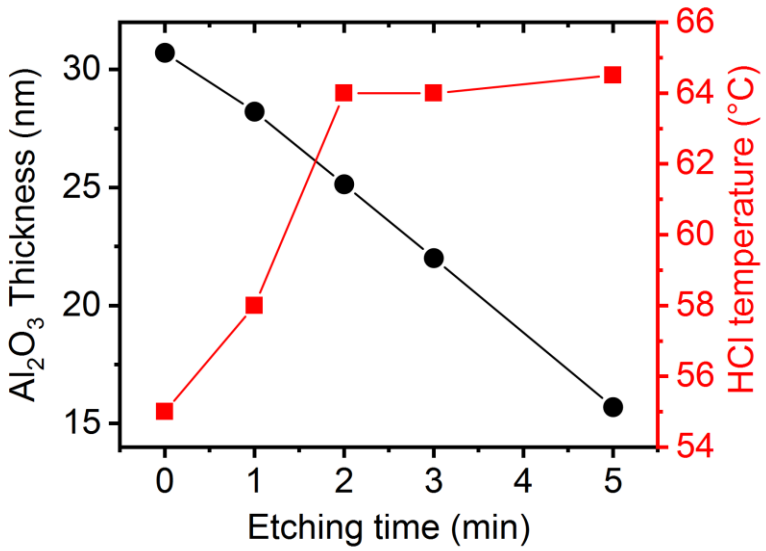


Figure E.3. HCl etching test on ALD Al_2O_3.

E.2 Process checking by SEM

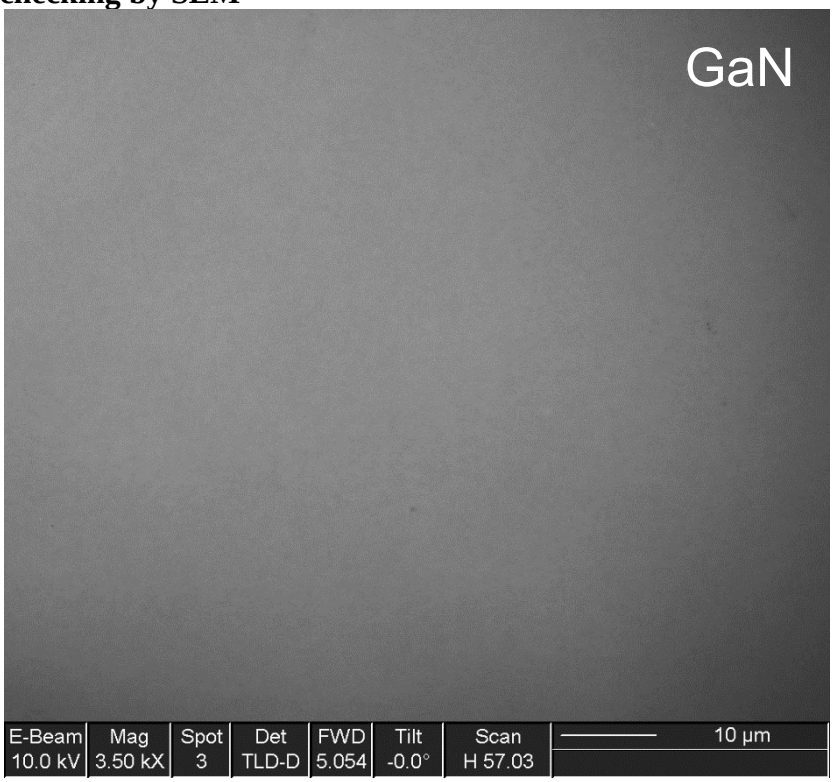


Figure E.4. Pre-processing: clean surface

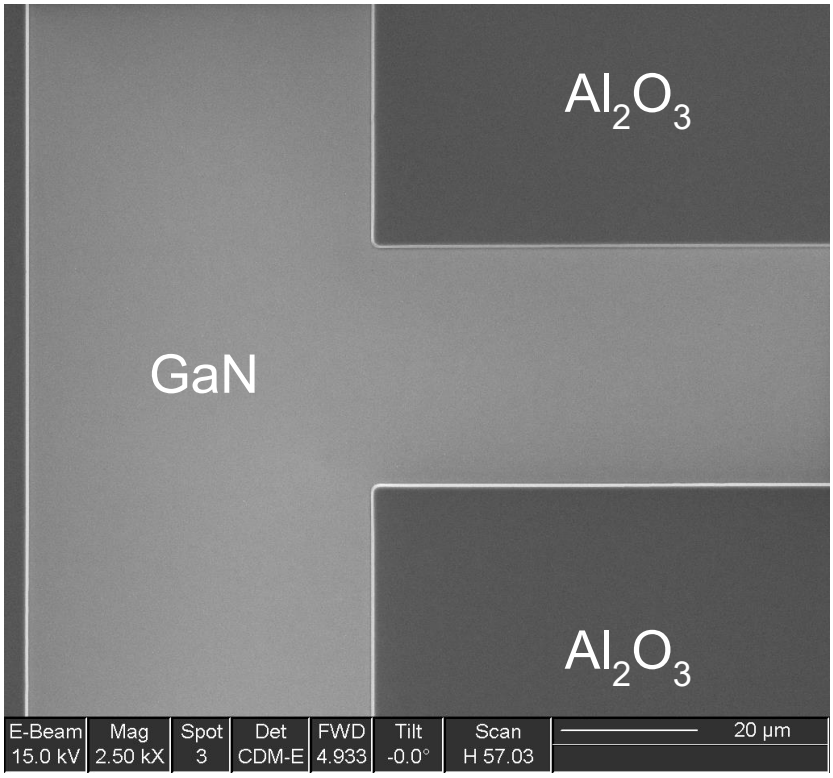


Figure E.5. Post-mesa-isolation PR removal.

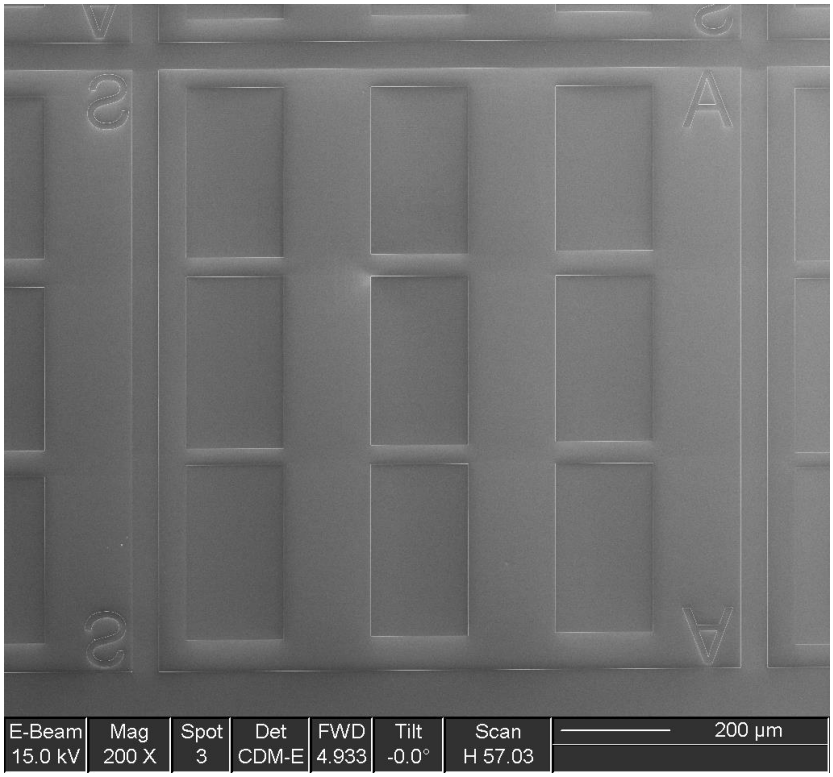


Figure E.6. Post-mesa-isolation PR removal.

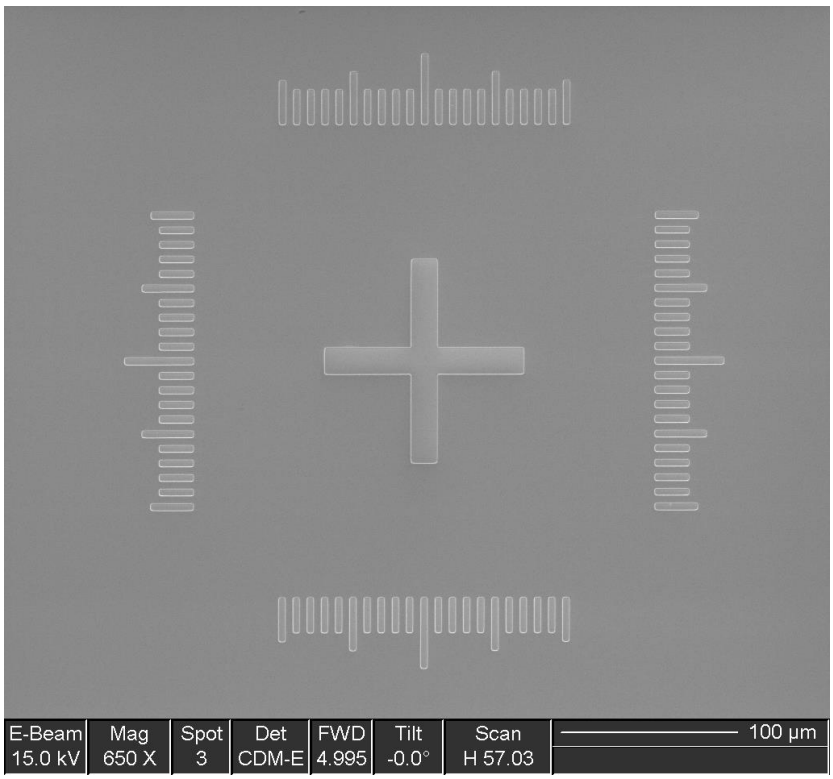


Figure E.7. Post-mesa-isolation PR removal.

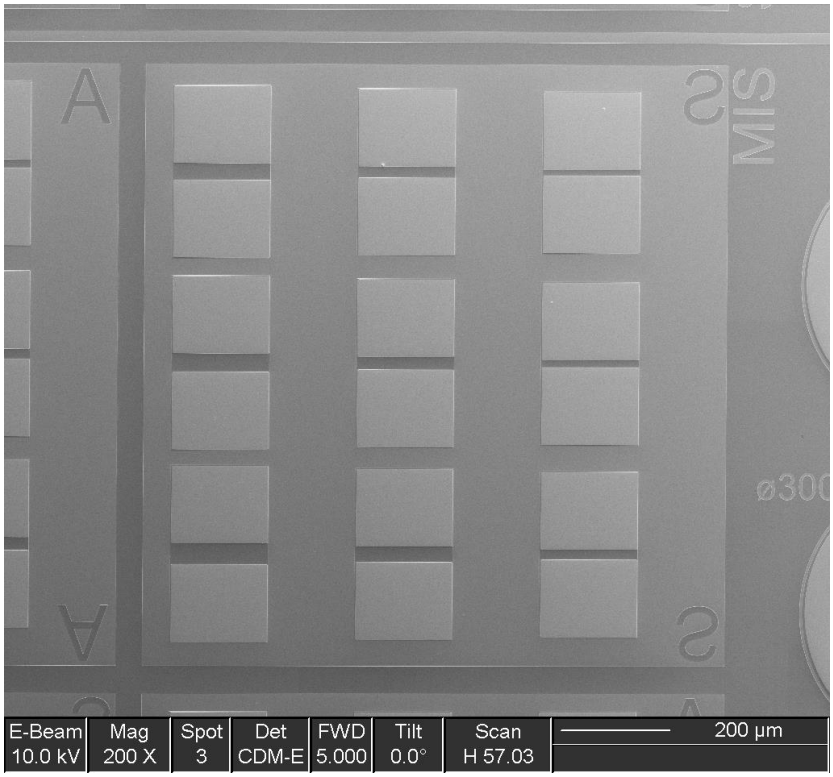


Figure E.8. Post-ohmic-contact-liftoff PR removal.

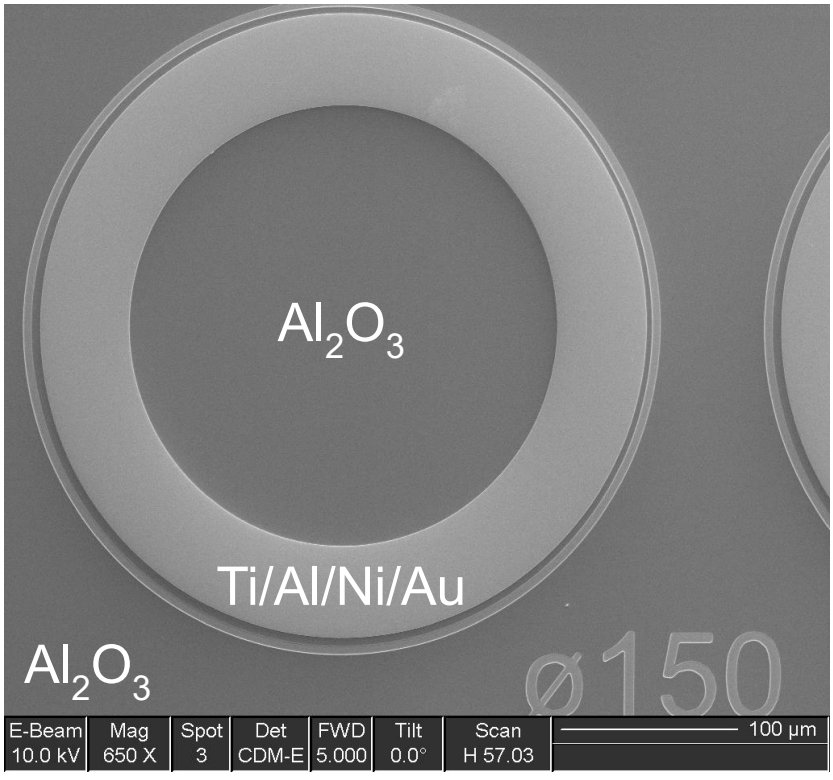


Figure E.9. Post-ohmic-contact-liftoff PR removal.

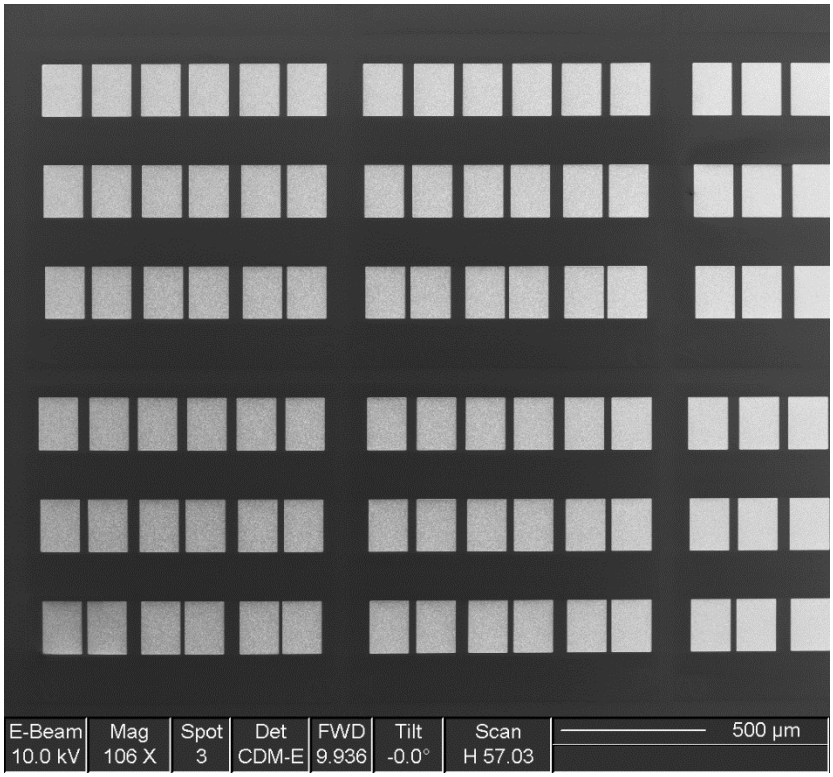


Figure E.10. Post-ohmic-contact rapid thermal annealing.

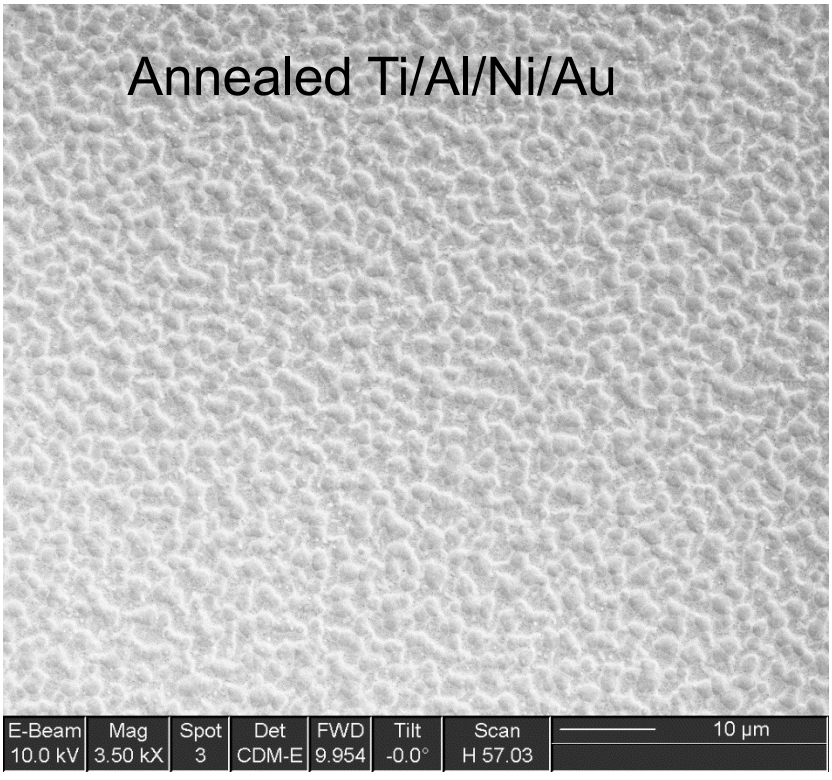


Figure E. 11. Post-ohmic-contact rapid thermal annealing.

APPENDIX F EQUIPMENT AND OPERATION PARAMETERS

F.1 Atomic layer deposition: Savannah atomic layer deposition

a. Available materials: Al_2O_3 and HfO_2

b. Temperature: 250°C (for Al_2O_3)

c. Deposition rate: 0.9 Å/cycle (for Al_2O_3)

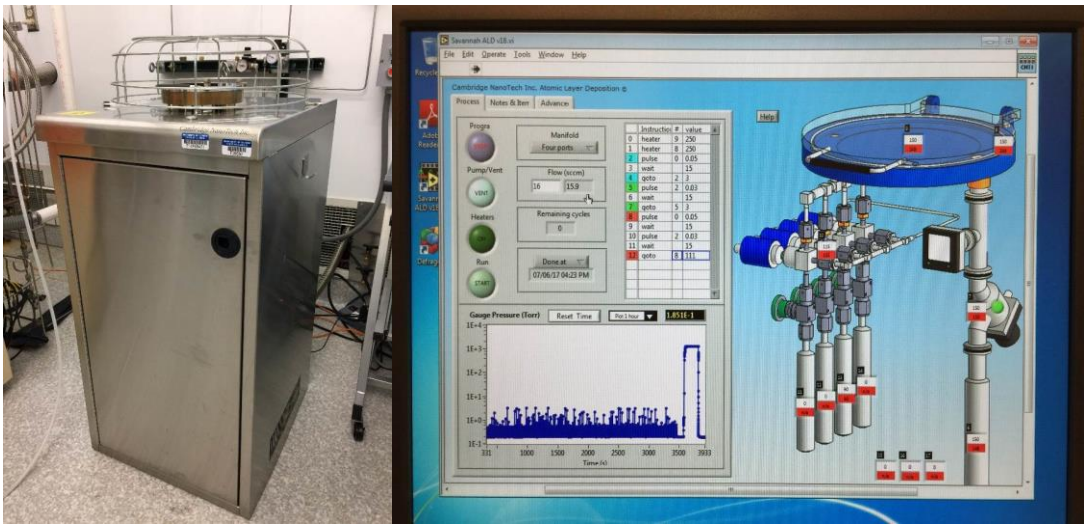


Figure F.1. Atomic layer deposition equipment and user interface.

F.2 Aligner for photolithography: Karl Suss MJB3 aligner

a. UV light source: options of 365 nm and 320 nm (9 mW/cm^2)

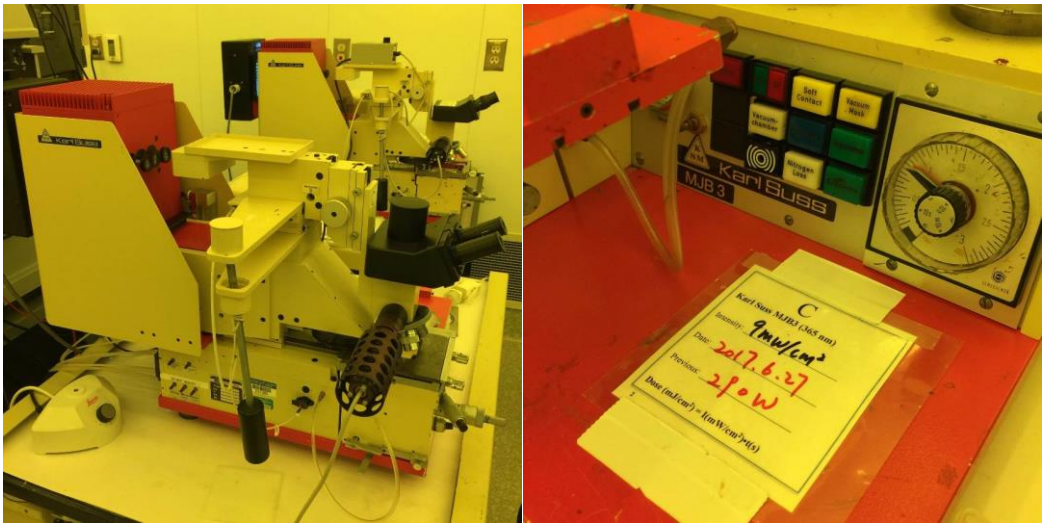


Figure F.2. UV lithography equipment and control panel.

F.3 O_2 plasma descum/ashing: Diener O_2 plasma chamber

a. Used recipe: 150 mTorr, 250 W, for 1 min

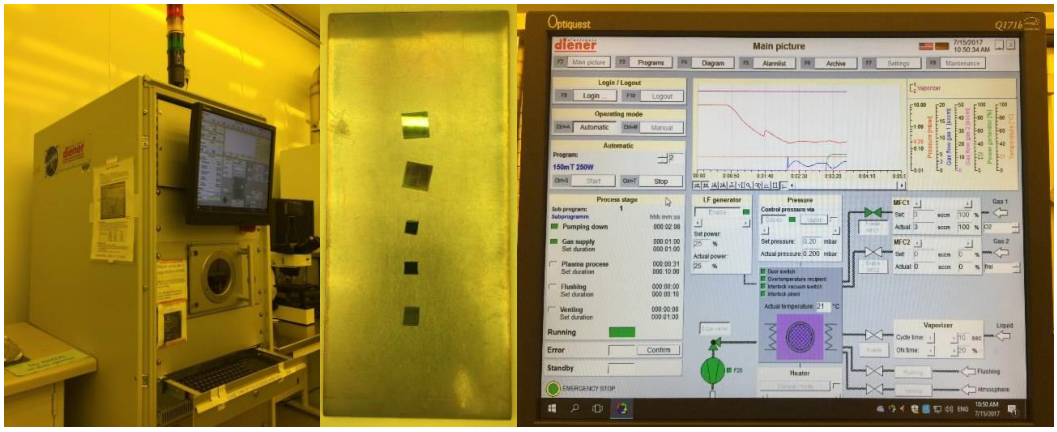


Figure F.3. O_2 plasma descum equipment and user interface.

F.4 Chlorine-based ICPRIE: OXFORD Plasmalab System100

a. Available gases: $SiCl_4$, BCl_3, Cl_2, CH_4, Ar, O_2, H_2, and SF_6 (for cleaning)

Figure F.4. ICPRIE equipment and user interface.

F.5 Electron beam evaporation: Temescal FC-2000

a. Used metals: Ti, Al, Ni, and Au

b. Pressure at the metal source: < 2.5×10^{-6} Torr

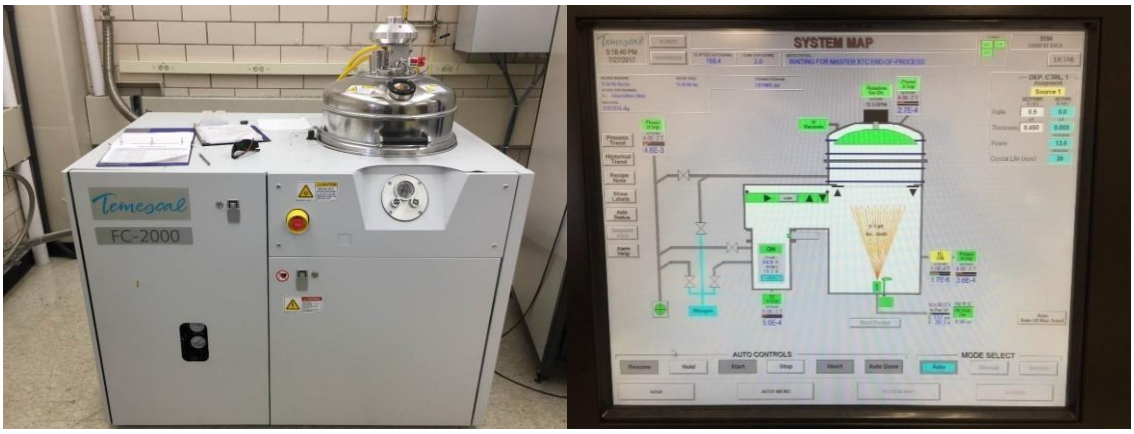


Figure F.5. Electron beam evaporation equipment and user interface.

F.6 Rapid thermal annealing: AG 610 rapid thermal processor

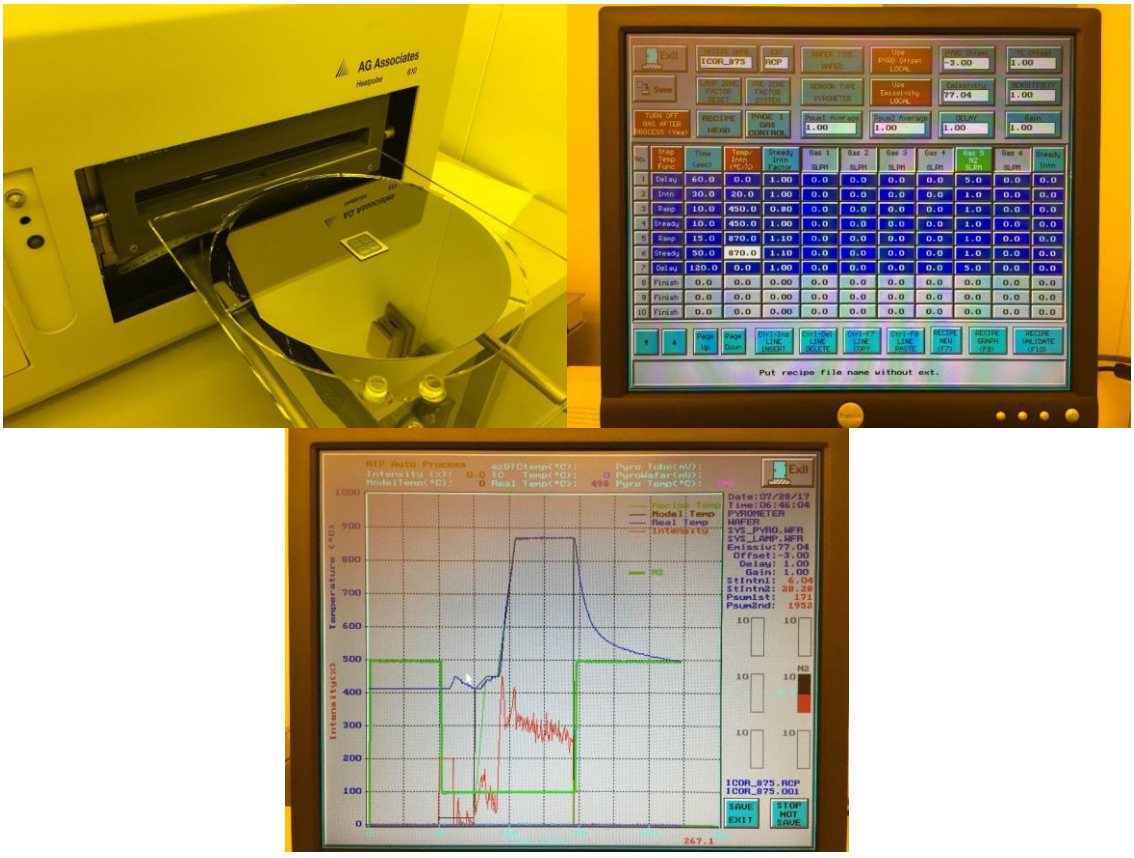


Figure F.6. Rapid thermal annealing equipment and user interface.

F.7 Electrical testing: Keithley 4200A-SCS parameter analyzer

a. Available modules: I-V source measurement unit (SMU) (channel 1, 2, and 3) and C-V multi-frequency capacitance unit (CVU) (1 kHz - 10 MHz) (channel 2, 3, and 4)

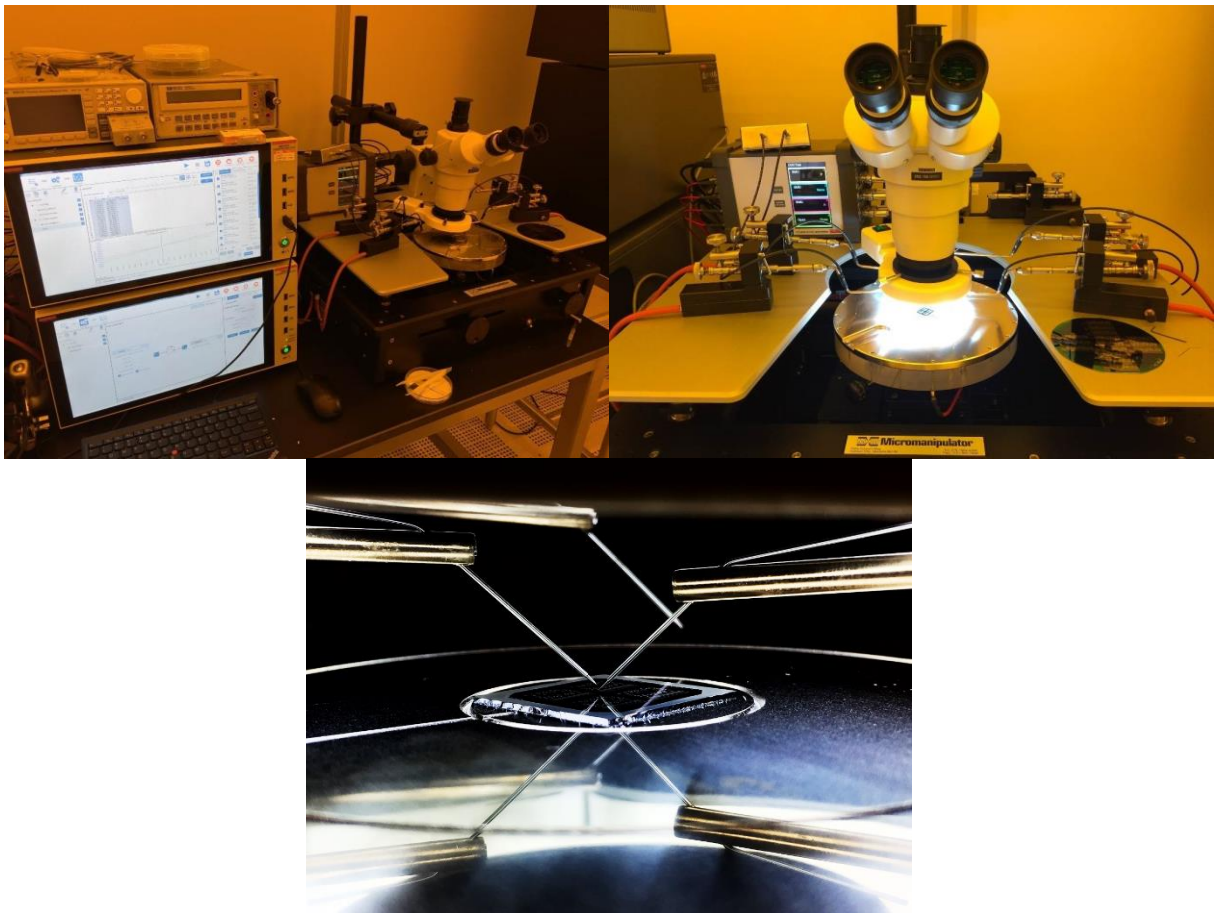


Figure F.7. Device electrical testing station.

F.8 Electrical testing: Probe station with water-cooling heating chuck

a. Keithley 4200A-SCS Parameter Analyzer

b. Temperature range: room temperature to 399°C

Figure F.8. Heating chuck and control panel for device electrical testing.

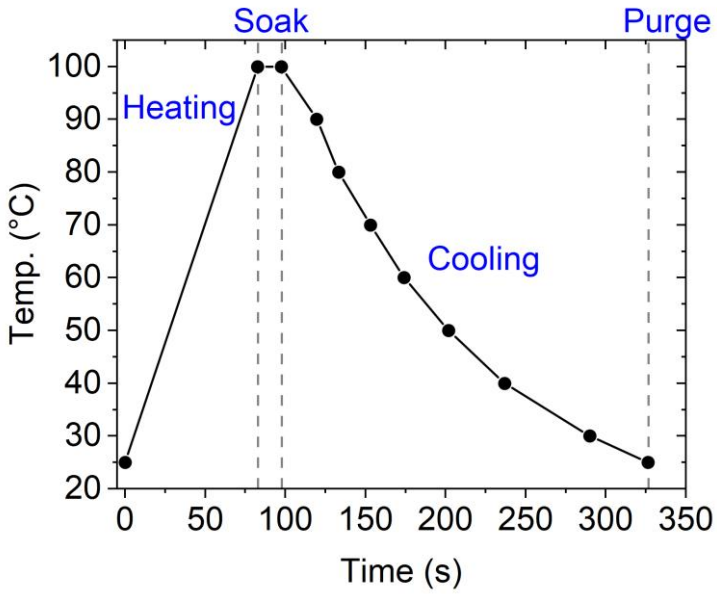


Figure F.9. Heating and water-cooling temperature profile.

F.9 Wire-bonding: K&S 4524A, 25-µm gold wire ball bonder

a. Capillary used: GAISER 1513-18-625GM (purchased from MRL)

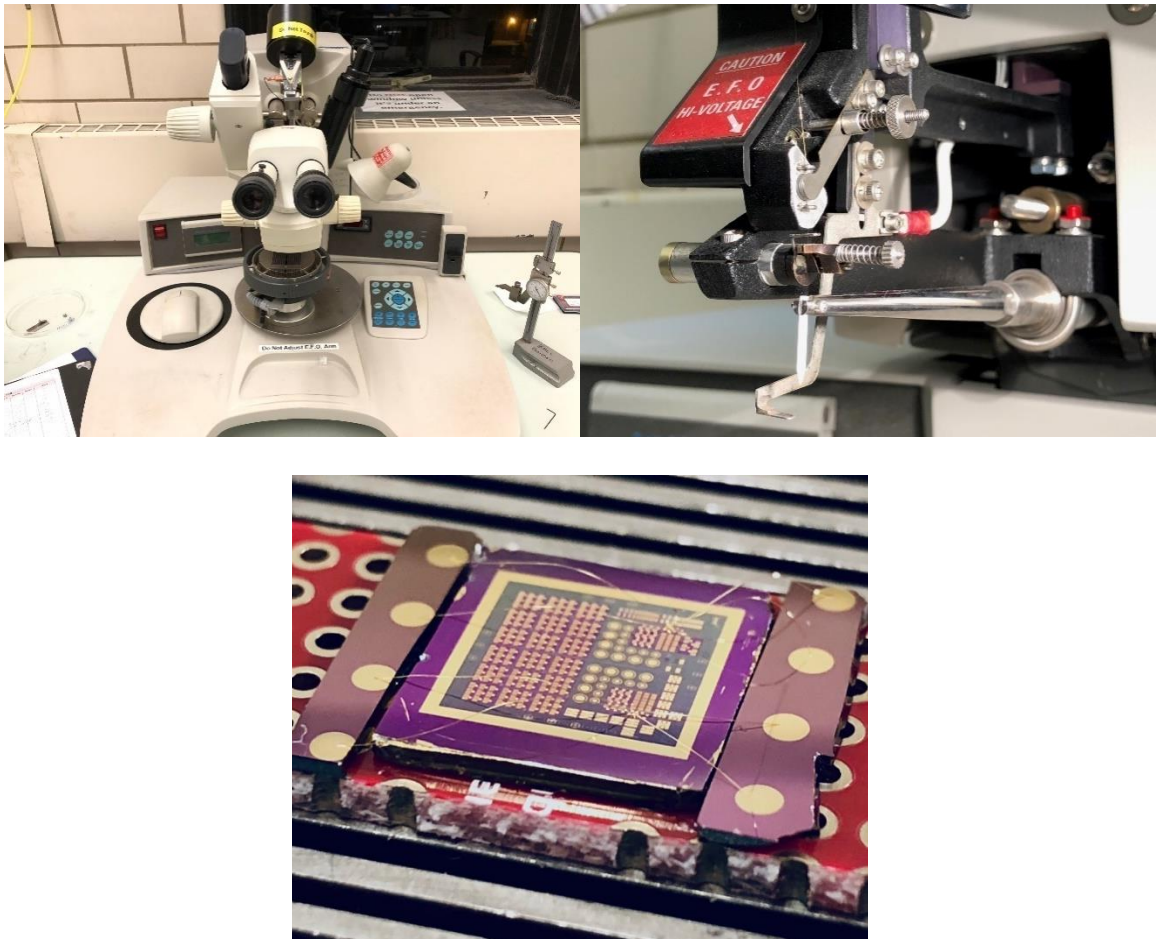


Figure F.10. Gold wire bonding station.

Table F.1. Bonding recipe for room-temperature gold-to-gold wire bonding.

General parameters	value	
Loop	4.0	
Tail	5.0	
Ball size	4.5	
Step	3.0	
Kink	2.0	
Bonding parameters	**1st bond**	**2nd bond**
Bonding type	Ball bond	Wedge bond
Search height	1.2	1.2
Power	1.5	2.5
Time	3.0	6.0
Force	1.8	5.0

APPENDIX G PROCESSING CHEMICAL COMPATIBILITY TABLE

Table G.1. Processing chemical compatibility table.

#	Process	Step	Used chemicals	Target Materials	Exposed Materials	Existing materials	Structural cross section
1	GaN surface preparation	degreasing	Toluene, acetone, methanol, DI	GaN	GaN	GaN	GaN/AlGaN/AlN (~20 nm) GaN (~1200 nm)
		treatment	HCl, NH_4OH, $(NH_4)_2S$	GaN	GaN	GaN	
2	GaN surface passivation	ALD Al_2O_3	TMA, DI		GaN	GaN	
3	Mesa isolation	Photolithography 1	HMDS, AZ5214, MIF917		Al_2O_3	Al_2O_3, GaN	
		Wet etching	BOE (HF, $(NH_4)F$)	Al_2O_3	PR, Al_2O_3, *GaN	PR, Al_2O_3, GaN	
		ICPRIE	Cl_2, BCl_3	GaN	PR, GaN	PR, Al_2O_3, GaN	
		PR removal	AZ400T (NMP, TMAH)	PR	PR, Al_2O_3, GaN	PR, Al_2O_3, GaN	
		degreasing	Toluene, acetone, methanol, DI	GaN, Al_2O_3	Al_2O_3, GaN	Al_2O_3, GaN	
4	S/D region opening	Photolithography 2	HMDS, AZ5214, MIF917		Al_2O_3, GaN	Al_2O_3, GaN	
		Wet etching	BOE (HF, $(NH_4)F$)	Al_2O_3	PR, Al_2O_3, *GaN	PR, Al_2O_3, GaN	
		PR removal	AZ400T (NMP, TMAH)	PR	PR, Al_2O_3, GaN	PR, Al_2O_3, GaN	
		degreasing	Toluene, acetone, methanol, DI	Al_2O_3, GaN	Al_2O_3, GaN	Al_2O_3, GaN	
5	S/D metallization	Photolithography 3	HMDS, AZ5214, MIF917		Al_2O_3, GaN	Al_2O_3, GaN	
		Hot HCl rinsing	HCl, DI	GaN	PR, GaN	PR, Al_2O_3, GaN	
		Ebeam evaporation	Ti/Al/Ni/Au	GaN	PR, GaN	PR, Al_2O_3, GaN	
		Lift-off	acetone, AZ400T, DI	PR	S/D metal, PR, Al_2O_3, GaN	S/D metal, PR, Al_2O_3, GaN	
6	Rapid thermal annealing			S/D metal	S/D metal, Al_2O_3, GaN	S/D metal, Al_2O_3, GaN	
7	S/D metal protection (Au deposition) (against BOE in process #16)	Photolithography 4	HMDS, AZ5214, MIF917		S/D metal, Al_2O_3, GaN	S/D metal, Al_2O_3, GaN	

Table G.1 (continued). Processing chemical compatibility table.

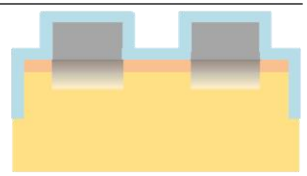
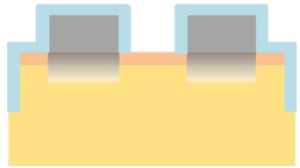
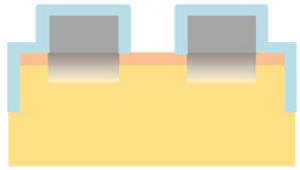
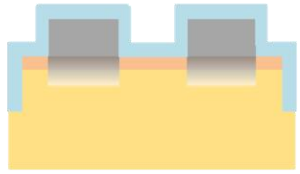
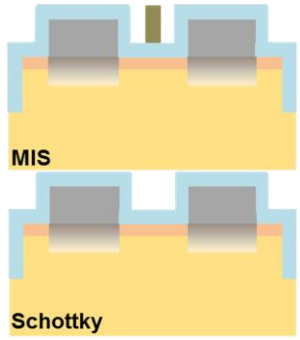
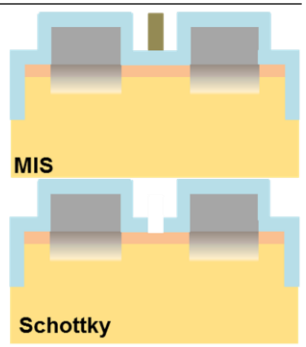
8	S/D metal protection (dummy Al2O3) (against chemicals for GaN surface treatments in process #10)	ALD Al_2O_3	TMA, DI		S/D metal, GaN	S/D metal, GaN	
9	GaN surface treatment window opening	Photolithography 5	HMDS, AZ5214, MIF917		S/D metal, Al_2O_3, GaN	S/D metal, Al_2O_3, GaN	
		Wet etching	BOE (HF, $(NH_4)F$)	Al_2O_3	PR, Al_2O_3, *GaN	PR, S/D metal, Al_2O_3, GaN	
		PR removal	AZ400T (NMP, TMAH)	PR	PR, S/D metal, Al_2O_3, GaN	PR, S/D metal, Al_2O_3, GaN	
10	GaN surface preparation	degreasing	Toluene, acetone, methanol, DI	Al_2O_3, GaN	Al_2O_3, GaN	S/D metal, Al_2O_3, GaN	
		treatment	HCl, NH_4OH, $(NH_4)_2S$	GaN	Al_2O_3, GaN	S/D metal, Al_2O_3, GaN	
11	Real GaN surface passivation	ALD Al_2O_3	TMA, DI		Al_2O_3, GaN		
12	MIS gate deposition	Photolithography 6	HMDS, AZ5214, MIF917		Al_2O_3, GaN	S/D metal, Al_2O_3, GaN	
		Ebeam evaporation	Ni/Au	Al_2O_3	PR, Al_2O_3	PR, S/D metal, Al_2O_3, GaN	
		Lift-off	acetone, AZ400T, DI	PR	MIS gate metal, PR, S/D metal, Al_2O_3, GaN	MIS gate metal, PR, S/D metal, Al_2O_3, GaN	

Table G.1 (continued). Processing chemical compatibility table.

13	**Schottky gate opening**	Photolithography 7	HMDS, AZ5214, MIF917		MIS gate metal, S/D metal, Al_2O_3, GaN	MIS gate metal, S/D metal, Al_2O_3, GaN	
		Wet etching	BOE (HF, $(NH_4)F$)	Al_2O_3	PR, Al_2O_3, *GaN	MIS gate metal, PR, S/D metal, Al_2O_3, GaN	
		PR removal	AZ400T (NMP, TMAH)	PR	MIS gate metal, PR, S/D metal, Al_2O_3, GaN	MIS gate metal, PR, S/D metal, Al_2O_3, GaN	
		degreasing	Toluene, acetone, methanol, DI	MIS gate metal, S/D metal, Al_2O_3, GaN	MIS gate metal, S/D metal, Al_2O_3, GaN	MIS gate metal, S/D metal, Al_2O_3, GaN	
14	**Schottky gate deposition**	Photolithography 8	HMDS, AZ5214, MIF917		MIS gate metal, S/D metal, Al_2O_3, GaN	MIS gate metal, S/D metal, Al_2O_3, GaN	
		Hot HCl rinsing	HCl, DI	GaN	PR, GaN	PR, MIS gate metal, S/D metal, Al_2O_3, GaN	
		Ebeam evaporation	Ni/Au	GaN	PR, GaN	PR, MIS gate metal, S/D metal, Al_2O_3, GaN	
		Lift-off	acetone, AZ400T, DI	PR	Schottky gate metal, PR, MIS gate metal, S/D metal, Al_2O_3, GaN	Schottky gate metal, PR, MIS gate metal, S/D metal, Al_2O_3, GaN	
15	**SiN passivation (optional)**						
16	**Contact opening**	Photolithography 9	HMDS, AZ5214, MIF917		Schottky gate metal, MIS gate metal, S/D metal, Al_2O_3	Schottky gate metal, MIS gate metal, S/D metal, Al_2O_3, GaN	
		Wet etching	BOE (HF, $(NH_4)F$)	Al_2O_3	PR, Schottky gate metal, MIS gate metal, S/D metal	PR, Schottky gate metal, MIS gate metal, S/D metal, Al_2O_3, GaN	

***Material exposed when step ends**

APPENDIX H PROCESSING LOG SHEET

Batch# ____	**Fabricated by _____**
Sample A	
Sample B	
Sample C	
Sample D	
Test Sample I	
Test Sample II	
Test Sample III	

#	Step	Date	Notes
0. Inspection			
	Surface check (Optical)	__/__/__	Inspection of surface crack
	Surface check (SEM)	__/__/__	Inspection of surface roughness (should be SEM flat)
	Cross section check (SEM)	__/__/__	Epilayer inspection
1. Surface cleaning and treatment. 2. 1st dummy ALD Al_2O_3 passivation			**Sample A B C D E** **Test sample I II III**
	Cleaning (Toluene, ACE, MET, MET, DI)	__/__/__	5 min on hotplate and 5 min in ultrasonic tank for each solvent
	Surface treatment (HCl, NH_4OH, $(NH_4)_2S$)	__/__/__	1 min 6% HCl (38% HCl : DI = 20 ml : 100 ml) at RT 1 min 7% NH_4OH (28% NH_4OH : DI = 30 ml: 90 ml) at RT 30 mins 5% $(NH_4)_2S$ (20% $(NH_4)_2S$: DI = 30 ml: 90 ml) at 50°C (1 min DI water rinse after each step)
	ALD Al_2O_3 passivation **(Real Samples and Test Samples)**	__/__/__	20 sec BOE on the test sample Si(111) to remove native oxide. ALD with recipe Al2O3 250°C Bayram for 100 cycles. Rate: ~1 Å/cycle.
3. Mesa isolation (Mask 1)			**Sample A B C D E** **Test sample I II III**
	Positive lithography Adhesion promotion with HMDS Photoresist: AZ5214e	__/__/__	2 min bakeout at 110°C 30 sec spin at 5000 rpm w/ 2500 rpm/s (HMDS applied first during spinning) 50 sec softbake at 100°C Edge bead removal 50 sec exposure with 320 nm UV light course (9 mW/cm^2) (last calibration time: __/__/__)
	Development	__/__/__	~ 30 sec in MIF 917 bath; 30 sec DI water rinse 50 sec hardbake at 110°C O_2 descum: 1 min w/ 250W at 150 mTorr
	Al_2O_3 wet etching	__/__/__	30 sec BOE and 30 sec DI water rinse
	Chlorine-based ICPRIE	__/__/__	1 min (150 W RIE 500 W ICP; 25 sccm BCl_3 10 sccm Cl_2;10mTorr)
	Photoresist removal (de-shell)	__/__/__	O_2 descum chamber cleaning: 10 min with 500 W at 150 mTorr O_2 descum: ___ min with 500 W at 150 mTorr Acetone rinse
	Photoresist removal (if necessary)	__/__/__	Clean with AZ400T-soaked Q-tip and 5 min AZ400T bath at 150°C Clean with AZ400T-soaked Q-tip and 5 min AZ400T bath at 150°C DI water rinse
	Cleaning (Toluene, ACE, MET, MET, DI)	__/__/__	5 min on hotplate and 5 min in ultrasonic tank for each solvent
4. Ohmic contact opening (Mask 2)			**Sample A B C D E** **Test sample I II III**
	Positive lithography Adhesion promotion with HMDS Photoresist: AZ5214e	__/__/__	2 min bakeout at 110°C 30 sec spin at 5000 rpm w/ 2500 rpm/s (HMDS applied first during spinning) 50 sec softbake at 100°C Edge bead removal 50 sec exposure with 320 nm UV light course (9 mW/cm^2) (last calibration time: __/__/__)

	Development	__/__/__	~ 30 sec in MIF 917 bath; 30 sec DI water rinse 50 sec hardbake at 110°C O_2 descum: 1 min w/ 250W at 150 mTorr
	Al_2O_3 wet etching	__/__/__	30 sec BOE and 30 sec DI water rinse
	Photoresist removal	__/__/__	Acetone rinse
	Photoresist removal (if necessary)	__/__/__	Clean with AZ400T-soaked Q-tip and 5 min AZ400T bath at 150°C Clean with AZ400T-soaked Q-tip and 5 min AZ400T bath at 150°C DI water rinse
	Cleaning (Toluene, ACE, MET, MET, DI)	__/__/__	5 min on hotplate and 5 min in ultrasonic tank for each solvent
5. Ohmic contact metallization (Mask 3)			**Sample A B C D E** **Test sample I II III**
	Negative lithography (image reversal) Adhesion promotion with HMDS Photoresist: AZ5214e	__/__/__	2 min bakeout at 110°C 30 sec spin at 5000 rpm w/ 2500 rpm/s (HMDS applied first during spinning) 60 sec softbake at 110°C Edge bead removal 5 sec exposure with 320 nm UV light course (9 mW/cm^2) (last calibration time: __/__/__) 60 sec post-exposure-bake at 110°C 2.3 min flood exposure with 320 nm UV light course (9 mW/cm^2)
	Development	__/__/__	~ 15 sec in MIF 917 bath; 30 sec DI water rinse *Use Q-tip soaked with PR to fully brush the uncovered dummy area (including the square boundary) 45 sec hardbake at 100°C O_2 descum: 1 min w/ 250W at 150 mTorr
	Hot HCl pre-metallization treatment	__/__/__	60 sec HCl : DI (1:1) at 150°C, DI water rinse
	Metallization	__/__/__	Ti (0.2 kÅ) / Al (1.2 kÅ) / Ni (0.55 kÅ) / Au (0.45 kÅ)
	Lift-off	__/__/__	ACE spray, 150°C AZ400T bath for 5 min, DI water bath for 10 min
	Cleaning (Toluene, ACE, MET, MET, DI)	__/__/__	5 min on hotplate and 5 min in ultrasonic tank for each solvent
*Avoid unwanted metal deposition on the dummy area that will NOT be covered by PR later on and then be attacked by BOE, contaminating the entire sample			
6. Rapid thermal annealing			**Sample A B C D E** **Test sample I II III**
	RTA **(Real Samples and Test Samples)**	__/__/__	Use our own 4" Si wafer Recipe: three-step annealing (3 min at 450°C, 40 sec at 700°C, and then 40 sec at 900°C)
7. Ohmic contact protection (Mask 4): using Au to protect annealed ohmic contact from BOE			**Sample A B C D E** **Test sample I II III**
	Negative lithography (image reversal) Adhesion promotion with HMDS Photoresist: AZ5214e	__/__/__	2 min bakeout at 110°C 30 sec spin at 5000 rpm w/ 2500 rpm/s (HMDS applied first during spinning) 60 sec softbake at 110°C Edge bead removal 5 sec exposure with 320 nm UV light course (9 mW/cm^2) (last calibration time: __/__/__) 60 sec post-exposure-bake at 110°C 2.3 min flood exposure with 320 nm UV light course (9 mW/cm^2)

	Development	__/__/__	~ 15 sec in MIF 917 bath; 30 sec DI water rinse *Use Q-tip soaked with PR to fully brush the uncovered dummy area (including the square boundary) 45 sec hardbake at 100°C O_2 descum: 1 min w/ 250W at 150 mTorr
	Metallization	__/__/__	Au (1 kÅ)
	Lift-off	__/__/__	ACE spray, 150°C AZ400T bath for 5 min, DI water bath for 10 min
	Cleaning (Toluene, ACE, MET, MET, DI)	__/__/__	5 min on hotplate and 5 min in ultrasonic tank for each
*Avoid unwanted metal deposition on the dummy area that will NOT be covered by PR later on and then be attacked by BOE, contaminating the entire sample			
8. 2nd Dummy ALD Al_2O_3			
	ALD Al_2O_3 passivation **(Real Samples and Test Samples)**	__/__/__	20 sec BOE on the test sample Si(111) to remove native oxide. ALD with recipe Al2O3 250°C Bayram for 100 cycles. Rate: ~1 Å/cycle.
9. Dummy Al_2O_3 removal (Mask 5)			**Sample A B C D E** **Test sample I II III**
	Positive lithography Adhesion promotion with HMDS Photoresist: AZ5214e	__/__/__	2 min bakeout at 110°C 30 sec spin at 5000 rpm w/ 2500 rpm/s (HMDS applied first during spinning) 50 sec softbake at 100°C Edge bead removal 50 sec exposure with 320 nm UV light course (9 mW/cm^2) (last calibration time: __/__/__)
	Development	__/__/__	~ 30 sec in MIF 917 bath; 30 sec DI water rinse *Use Q-tip soaked with PR to fully brush the uncovered S/D metal in the dummy area (if any) 50 sec hardbake at 110°C O_2 descum: 1 min w/ 250W at 150 mTorr
	Al_2O_3 wet etching	__/__/__	30 ~ 40 sec BOE and 30 sec DI water rinse
	Photoresist removal	__/__/__	Acetone rinse
	Photoresist removal (if necessary)	__/__/__	Clean with AZ400T-soaked Q-tip and 5 min AZ400T bath at 150°C Clean with AZ400T-soaked Q-tip and 5 min AZ400T bath at 150°C DI water rinse
	Cleaning (Toluene, ACE, MET, MET, DI)	__/__/__	5 min on hotplate and 5 min in ultrasonic tank for each solvent
10. GaN surface treatment			
	Surface treatment (HCl, NH_4OH, $(NH_4)_2S$)	__/__/__	1 min 6% HCl (38% HCl : DI = 20 ml : 100 ml) at RT 1 min 7% NH_4OH (28% NH_4OH : DI = 30 ml: 90 ml) at RT 30 mins 5% $(NH_4)_2S$ (20% $(NH_4)_2S$: DI = 30 ml: 90 ml) at 50°C (1 min DI water rinse after each step)
11. Real ALD Al_2O_3			**Sample A B C D E** **Test sample I II III**
	ALD Al_2O_3 passivation **(Real Samples and Test Samples)**	__/__/__	20 sec BOE on the test sample Si(111) to remove native oxide.

			ALD with recipe Al2O3 250°C Bayram for 100 cycles. Rate: ~1 Å/cycle.
12. MIS gate deposition (Mask 6)			
	Negative lithography (image reversal) Adhesion promotion with HMDS Photoresist: AZ5214e	__/__/__	2 min bakeout at 110°C 30 sec spin at 5000 rpm w/ 2500 rpm/s (HMDS applied first during spinning) 60 sec softbake at 110°C Edge bead removal 5 sec exposure with 320 nm UV light course (9 mW/cm^2) (last calibration time: __/__/__) 60 sec post-exposure-bake at 110°C 2.3 min flood exposure with 320 nm UV light course (9 mW/cm^2)
	Development	__/__/__	~ 15 sec in MIF 917 bath; 30 sec DI water rinse *Use Q-tip soaked with PR to fully brush the uncovered dummy area 45 sec hardbake at 100°C O_2 descum: 1 min w/ 250W at 150 mTorr
	Metallization	__/__/__	Ni (0.2 kÅ) / Au (2 kÅ)
	Lift-off	__/__/__	ACE spray, 150°C AZ400T bath for 5 min, DI water bath for 10 min
	Cleaning (Toluene, ACE, MET, MET, DI)	__/__/__	5 min on hotplate and 5 min in ultrasonic tank for each
13. Schottky gate opening (Mask 7)			**Sample A B C D E** **Test sample I II III**
	Positive lithography Adhesion promotion with HMDS Photoresist: AZ5214e	__/__/__	2 min bakeout at 110°C 30 sec spin at 5000 rpm w/ 2500 rpm/s (HMDS applied first during spinning) 50 sec softbake at 100°C Edge bead removal 50 sec exposure with 320 nm UV light course (9 mW/cm^2) (last calibration time: __/__/__)
	Development	__/__/__	~ 30 sec in MIF 917 bath; 30 sec DI water rinse *Use Q-tip soaked with PR to fully brush the uncovered S/D metal in the dummy area (if any) 50 sec hardbake at 110°C O_2 descum: 1 min w/ 250W at 150 mTorr
	Al_2O_3 wet etching	__/__/__	30 ~ 40 sec BOE and 30 sec DI water rinse
	Photoresist removal	__/__/__	Acetone rinse
	Photoresist removal (if necessary)	__/__/__	Clean with AZ400T-soaked Q-tip and 5 min AZ400T bath at 150°C Clean with AZ400T-soaked Q-tip and 5 min AZ400T bath at 150°C DI water rinse
	Cleaning (Toluene, ACE, MET, MET, DI)	__/__/__	5 min on hotplate and 5 min in ultrasonic tank for each solvent
14. Schottky gate metallization (Mask 8)			
	Negative lithography (image reversal) Adhesion promotion with HMDS Photoresist: AZ5214e	__/__/__	2 min bakeout at 110°C 30 sec spin at 5000 rpm w/ 2500 rpm/s (HMDS applied first during spinning) 60 sec softbake at 110°C Edge bead removal 5 sec exposure with 320 nm UV light course (9 mW/cm^2) (last calibration time: __/__/__)

			60 sec post-exposure-bake at 110°C 2.3 min flood exposure with 320 nm UV light course (9 mW/cm^2)
	Development	__/__/__	~ 15 sec in MIF 917 bath; 30 sec DI water rinse *Use Q-tip soaked with PR to fully brush the uncovered dummy area 45 sec hardbake at 100°C O_2 descum: 1 min w/ 250W at 150 mTorr
	Metallization	__/__/__	Ni (0.2 kÅ) / Au (2 kÅ)
	Lift-off	__/__/__	ACE spray, 150°C AZ400T bath for 5 min, DI water bath for 10 min
	Cleaning (Toluene, ACE, MET, MET, DI)	__/__/__	5 min on hotplate and 5 min in ultrasonic tank for each
15. PECVD SiN_x passivation (optional)			**Sample A B C D E** **Test sample I II III**
16. Contact opening (Mask 9)			
	Positive lithography Adhesion promotion with HMDS Photoresist: AZ5214e	__/__/__	2 min bakeout at 110°C 30 sec spin at 5000 rpm w/ 2500 rpm/s (HMDS applied first during spinning) 50 sec softbake at 100°C Edge bead removal 50 sec exposure with 320 nm UV light course (9 mW/cm^2) (last calibration time: __/__/__)
	Development	__/__/__	~ 30 sec in MIF 917 bath; 30 sec DI water rinse *Use Q-tip soaked with PR to fully brush the uncovered S/D metal in the dummy area (if any) 50 sec hardbake at 110°C O_2 descum: 1 min w/ 250W at 150 mTorr
	Al_2O_3 wet etching	__/__/__	30 ~ 40 sec BOE and 30 sec DI water rinse
	Photoresist removal	__/__/__	Acetone rinse
	Photoresist removal (if necessary)	__/__/__	Clean with AZ400T-soaked Q-tip and 5 min AZ400T bath at 150°C Clean with AZ400T-soaked Q-tip and 5 min AZ400T bath at 150°C DI water rinse
	Cleaning (Toluene, ACE, MET, MET, DI)	__/__/__	5 min on hotplate and 5 min in ultrasonic tank for each solvent

APPENDIX I RF MEASUREMENT, TRANSISTOR PARAMETER EXTRACTION, AND DE-EMBEDDING METHODS

I.1 RF Measurement

Device electrical testing at different frequency regimes requires different measurement procedures. In low-frequency regime, generally function generator, voltmeter, and current meter will suffice since compared to the device dimension, the relative long wavelength of the signal results in current and voltage that can be treated as constants (lumped element model). However, in high-frequency regime, due to the extremely short wavelength, complex nature of the device/circuit components, non-negligible phase difference between current and voltage, and transmission line effects, direct measurement and analysis using waves of current and voltage become unrealistic. Instead, electrical power waves are constant and are therefore commonly used. While the electrical power waves (EM waves) are traveling, a certain voltage (from electric field) and current (from magnetic field) relation is imposed by the electrical property of the transmission line. Once an electrical power wave (incident wave) encounters an obstacle (mismatched impedance) along the transmission line, a reflected wave (scattered wave) and a transmitted wave can result. The ratio of the reflected and incident power waves is defined as reflection coefficient, which is also known as scattering (S-) parameter. Scattering parameter is in a complex form that carries both magnitude and phase information and can therefore be used to provide complete insight into the linear behavior of RF components/systems.

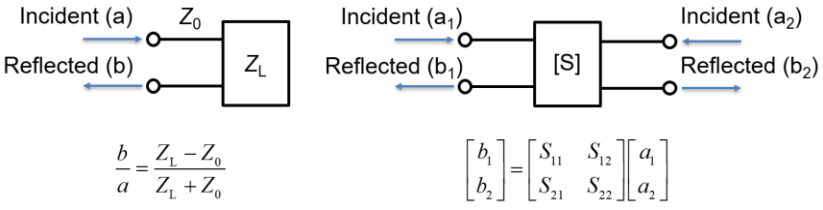


Figure I.1. Reflection coefficient and scattering parameters. [Fundamentals of Vector Network Analysis Primer, Rohde & Schwarz USA, Inc.].

In order to measure S-parameters of RF components/systems, vector network analyzer (VNA) is commonly used. Compared to scalar network analyzer, VNA measures both magnitude and phase of electrical power waves. It stimulates an RF network at a given port with a continuous electrical power wave signal and then measures the incident and reflected waves at all ports that are terminated with specific load impedances, typically 50 Ω. A standard VNA N-port block diagram is shown below [*Fundamentals of Vector Network Analysis Primer*, Rohde & Schwarz USA, Inc.].

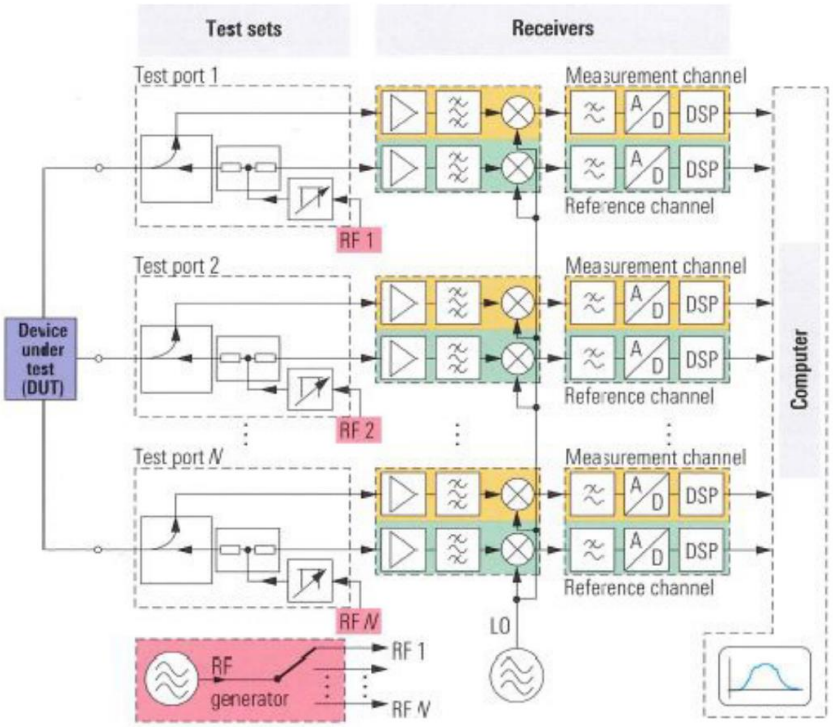


Figure I.2. Standard VNA N-port block diagram. [Fundamentals of Vector Network Analysis Primer, Rohde & Schwarz USA, Inc.].

Overall, the system is composed of three major parts: test sets, receivers, and computer. In the test sets, the device under test (DUT) is connected to signal-separation hardwares (directional couplers) that separate the reflected electrical power waves from the incident waves. Low coupling loss has to be achieved in order to assure accurate measurements. The RF generator possesses tunable output power and frequency and can rapidly sweep across intended frequencies in order to collect

the frequency response of the DUT. Then, all of the incident and reflected electrical power waves are fed into the receiver for extracting their respective magnitude and phase using heterodyne technique. A detailed heterodyne receiver block diagram is shown below [*Fundamentals of Vector Network Analysis Primer*, Rohde & Schwarz USA, Inc.].

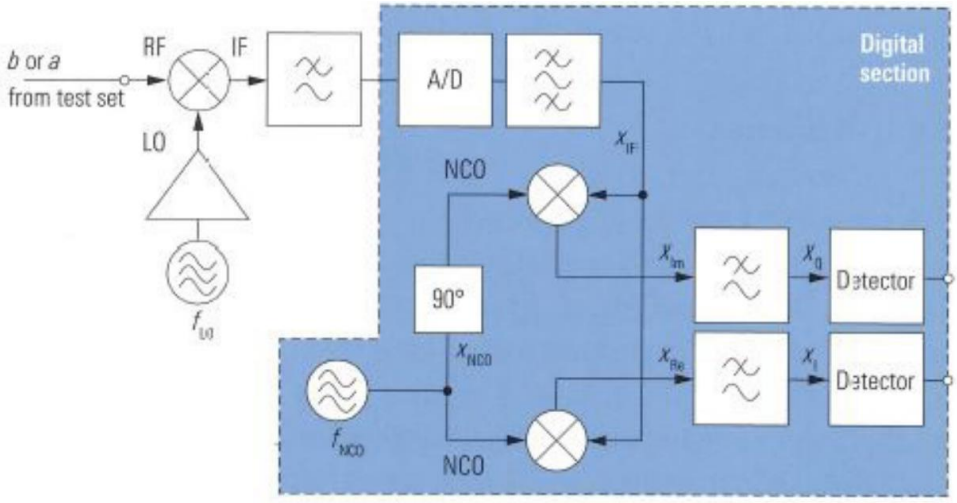


Figure I.3. Heterodyne receiver block diagram. [Fundamentals of Vector Network Analysis Primer, Rohde & Schwarz USA, Inc.].

The frequencies (f_{RF}) of an electrical power waves (either incident or reflected) will first be down-converted to intermediate frequency (f_{IM}) by the multiplier, the local oscillator (f_{LO}), and the low-pass filter for processing, while the information of magnitude and phase is still preserved. Note that while f_{RF} and f_{LO} can both be changed as needed, it is imperative to keep $f_{IM} = f_{RF} - f_{LO}$ as a fixed value for a reason that will be revealed later. The wave will then be passed through an A/D converter for the microprocessor to process, followed by a band-pass filter for better signal selectivity. Then, the wave will be fed into a quadrature demodulator (I/Q demodulator) to decouple the real and imaginary parts of the complex wave. The reason why the intermediate frequency f_{IM} has to be exactly equal to the frequency (f_{NCO}) of the numerically controlled oscillator (NCO) of the I/Q demodulator is that, after the followed low-pass filter, only constants that preserve the information of magnitude and phase will be kept, and they can then be used to extract

the magnitude and phase of the original electrical power wave through trigonometry theory. With all of the incident of reflected electrical power waves obtained, an S-parameter matrix that represents the DUT can then be established for further analysis.

I.2 Heterodyne: Detailed mathematical derivation

Let the original electrical power wave of interest (RF wave) and the LO wave be:

$$x_{\mathrm{RF}} = A\cos(2\pi f_{\mathrm{RF}} t + \phi)$$
$$x_{\mathrm{LO}} = B\cos(2\pi f_{\mathrm{LO}} t).$$

After the multiplier:

$$x_{\mathrm{RF}} \times x_{\mathrm{LO}} = \frac{AB}{2}\left\{\cos\left[2\pi\left(f_{\mathrm{RF}} + f_{\mathrm{LO}}\right)t + \phi\right] + \cos\left[2\pi\left(f_{\mathrm{RF}} - f_{\mathrm{LO}}\right)t + \phi\right]\right\}.$$

After the low-pass filter:

$$x_{\mathrm{IM}} = \frac{AB}{2}\cos\left[2\pi\left(f_{\mathrm{RF}} - f_{\mathrm{LO}}\right)t + \phi\right] = \frac{AB}{2}\cos\left[2\pi f_{\mathrm{IM}} t + \phi\right].$$

Let the NCO wave be:

$$x_{\mathrm{NCO}} = C\cos\left[2\pi f_{\mathrm{NCO}} t\right],$$

where $f_{\mathrm{NCO}} = f_{\mathrm{IM}}$.

After the I/Q demodulator, the real (x_{R}) and imaginary (x_{I}) parts of v_{IM} are then obtained as:

$$x_{\mathrm{IM,R}} = \frac{ABC}{4}\left[\cos(4\pi f_{\mathrm{IM}} t + \phi) + \cos(\phi)\right]$$
$$x_{\mathrm{IM,I}} = \frac{ABC}{4}\left[\sin(4\pi f_{\mathrm{IM}} t + \phi) - \sin(\phi)\right].$$

With the low-pass filter, we then have two constants (in-phase and quadrature components) as:

$$x_{\mathrm{I}} = \frac{ABC}{4}\cos(\phi)$$
$$x_{\mathrm{Q}} = \frac{ABC}{4}\sin(\phi).$$

Given that both B and C are known values, A and ϕ can then be deduced as:

$$A = \frac{4x_{\mathrm{I}}}{BC\cos(\phi)} = \frac{4x_{\mathrm{Q}}}{BC\sin(\phi)}$$

$$\phi = \tan^{-1}\left(\frac{x_{\mathrm{Q}}}{x_{\mathrm{I}}}\right),$$

respectively representing the magnitude and the phase of the original electrical power wave of interest. The computer then takes the information of all incident and reflected electrical power waves and produce the S-parameter matrix.

I.3 Transistor parameter extraction

Assuming a two-port network, the obtained S-parameter matrix can then be transformed into Y-parameter matrix (admittance parameters) for transistor parameter extraction:

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} = \begin{bmatrix} \dfrac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} & \dfrac{-2S_{12}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} \\ \dfrac{-2S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} & \dfrac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1+S_{11})(1+S_{22})-S_{12}S_{21}} \end{bmatrix},$$

where

$$g_{\mathrm{m}} = \mathrm{Re}(Y_{21})$$
$$C_{\mathrm{gs}} = \left[\mathrm{Im}(Y_{11}) + \mathrm{Im}(Y_{12})\right]/\omega$$
$$C_{\mathrm{gd}} = -\mathrm{Im}(Y_{12})/\omega$$
$$R_{\mathrm{g}} = \mathrm{Re}(Y_{11})/\mathrm{Im}(Y_{11})^2$$
$$C_{\mathrm{g}} = C_{\mathrm{gs}} + C_{\mathrm{gd}}$$
$$C_{\mathrm{ds}} = \left[\mathrm{Im}(Y_{22}) + \mathrm{Im}(Y_{12})\right]/\omega$$
$$g_{\mathrm{ds}} = \mathrm{Re}(Y_{22})$$
$$h_{21} = Y_{21}/Y_{11},\ h_{21}(f_{\mathrm{T}}) = 1$$
$$U = \frac{\left|Y_{21} - Y_{12}\right|^2}{4\left[\mathrm{Re}(Y_{11})\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12})\mathrm{Re}(Y_{21})\right]},\ U(f_{\max}) = 1.$$

I.4 De-embedding

When performing RF measurement using a VNA, calibration will have to be performed prior to the measurement in order to extend the reference plane far to the DUT, meaning that the parasitic components from the tool and cables will have to be compensated in order to reveal the actual parameters of the DUT. However, in high-frequency regime, even the probing pads and wires in the DUT can produce significant parasitic capacitance and resistance, rendering the extracted transistor parameters inaccurate. A typical lumped circuit model that includes these parasitic components can be illustrated in Figure I.4., where Y, Z, OP, and SH are admittance, impedance, open, and short, respectively.

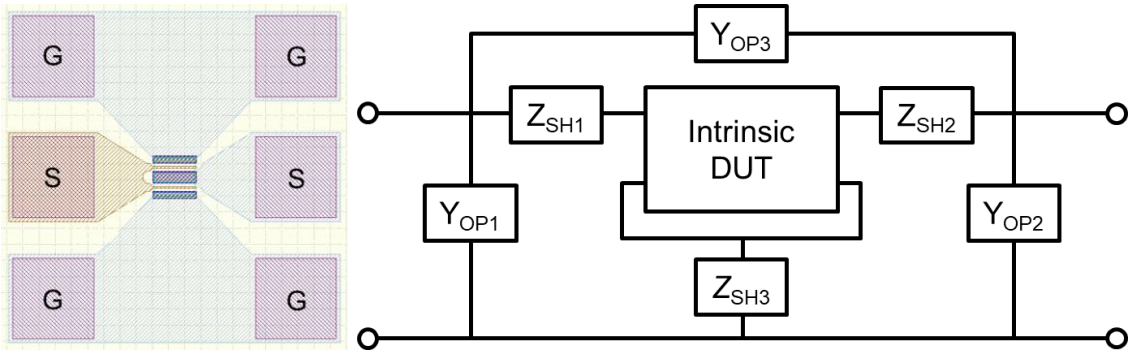


Figure I.4. Typical lumped circuit model of the DUT.

In order to extract the intrinsic DUT parameters, designs of respective patterns that can closely represent the parasitic admittances and impedances are required.

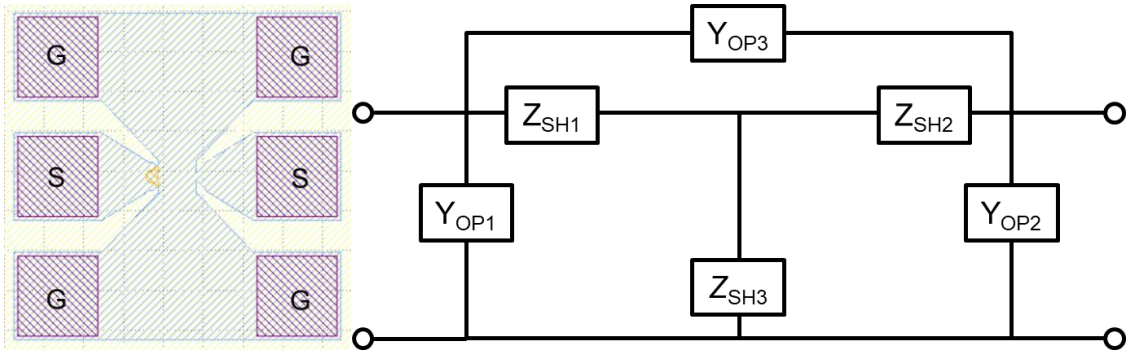


Figure I.5. Short circuit model where the intrinsic DUT is shorted.

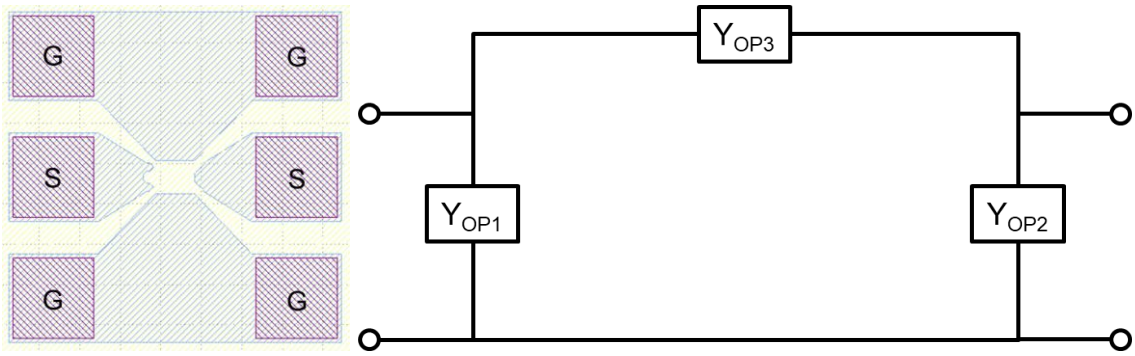


Figure I.6. Open circuit model where the intrinsic DUT is removed, leaving the circuit opened.

Radio-frequency measurements will be done individually on these patterns in order to produce the respective S-parameter matrixes and then Y-parameter matrixes. Finally, by performing the 2 by 2 matrix calculation using the equation

$$\left[Y_{\mathrm{DUT,intrinsic}}\right]=\left[\left[\left[Y_{\mathrm{DUT}}\right]-\left[Y_{\mathrm{OP}}\right]\right]^{-1}-\left[\left[Y_{\mathrm{SH}}\right]-\left[Y_{\mathrm{OP}}\right]\right]^{-1}\right]^{-1},$$

where

$$[Y]=[Z]^{-1},$$

one can extract the Y-parameter matrix of the intrinsic DUT and therefore the respective intrinsic transistor parameters. The aforementioned process is called de-embedding, or more specifically, open-short de-embedding. Depending on the complexity of the DUT structure, more advanced de-embedding methods might be needed. By performing a proper de-embedding, generally one can obtained improved f_T and f_{max}.