NORMALLY-OFF GAN HEMTS

By

Philip Tsai

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University of Illinois at Urbana-Champaign

Advisor: Can Bayram

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Abstract

As silicon transistors have become a staple in everyday usages, other semiconductor materials (specifically III-V materials) are being researched to determine how their differing physical properties can be harnessed toward even better devices or applications. Useful properties of the III-V semiconductor gallium nitride (GaN) compared to silicon are its larger bandgap energy, larger breakdown field, and higher thermal conductivity. These properties allow GaN transistors to more effectively be used as power switching devices with larger current density, switching speeds and better power efficiency than that of Si power devices. The GaN transistor structure used to create these power switching devices is the high electron mobility transistors (HEMT), which has a naturally conducting channel at the hetero-interface between GaN and $Al_xGa_{1-x}N$. Since the source/drain channel is conducting while the HEMT is at equilibrium, the device is considered a normally ON device where it takes no gate voltage for the transistor to have a drain current. This normally ON characteristic of the transistor, however, is a limitation of the device. For safety and OFF mode power saving concerns, it is ideal for the HEMT to be a normally OFF device where the channel is non-conducting with no gate bias. There have been many methods proposed to deplete the channel of its conductive properties and I believe that the pGaN gate method is the most promising. The pGaN gate method entails a gate made of heavily p-type doped GaN. This in turn lowers the equilibrium Fermi level enough to deplete the hetero-interface of a conducting channel. Using Synopsis TCAD simulation software, I created a pGaN gate HEMT structure and explored its normally OFF characteristics and limitations.

Subject Keywords: gallium nitride, high electron mobility transistors, enhancement mode, Synopsys TCAD

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Contents

1. Introduction

Transistors are micro/nano-sized electrical switches that are made of semiconductor material. These switches can be triggered by electric signals where the voltage signal tells the device whether to conduct or insulate electricity. There are two main types of transistors: field effect transistors (FET) and bipolar junction transistors (BJT). Transistors are used in almost every electronic device worldwide: from the processing chips in a smartphone to the circuits in a pacemaker. Their usage also spans many fields like sports, medicine, entertainment and education.

To give brief history of the transistor, in the early 1900s AT&T wanted a transcontinental phone service and a key to this was to build an effective signal amplifier. Around 1906, the only amplifier was Lee De Forest's vacuum tube triode; however, this amplifier was not ideal because vacuum tubes were extremely unreliable due to their giving off too much heat and consuming too much power [1].The solution was to design an amplifier made out of semiconductor materials. Bell Labs scientists were given the tasks to research solid state semiconductors for amplification and on December 16, 1947, John Bardeen and Walter Brattain built the first point-contact transistor while working at Bell Labs [1]. Furthermore in 1952, a radar scientist of the Royal Radar Establishment, Geoffrey Dummer, realized that every component of a circuit can be made from a single piece of semiconductor and in 1958, Jack Kilby of Texas Instruments followed this idea and came up with the invention of the integrated circuit on germanium. Robert Noyce of Fairchild Semiconductor improved upon Kilby's IC by making it on silicon [10].

Also in the 1950s, the BJT was developed. As time went on, there was a constant need to improve their power ratings and switching frequency as they were used for power applications [2].

By the 1970s, devices were greatly improved upon as knowledge of transistors increased. BJTs utilized 4-inch diameter wafer technology with a voltage rating of larger than 5000 V [2]. Power BJTs however at the time had troubles with cost effectiveness and efficiency due to low current gain and second breakdown failure modes. Due to these issues, the power MOSFET was introduced to replace the power BJT. The power MOSFET had high input impedance and switching speed, which is desired,

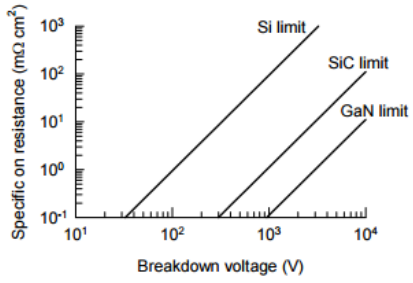

Figure 1: Specific on-resistance vs Breakdown voltage for different materials based on BFOM

but at the time it did not thrive in high voltage situations [2].

Around the 1980s, Jayant Baliga of GE introduced the insulated gate bipolar transistor (IGBT) which is a mix of BJT and MOSFET power devices for medium power electronic applications of voltages between 2,400 V - 69,000 V for nominal systems [11]. Benefits if the IGBT included high power gain, input impedance, switching speed and a large safe operating area (SOA) [3]. SOA is the space in an I-V curve where a device can operate without destructive failure [3]. Baliga also introduced the Baliga figure of merit (BFOM) which related on-resistance of the drift region of a certain material with the basic properties of that material such as the breakdown field.

The BFOM is significant because it provided information on devices when different materials were used to make up power devices. The BFOM made engineers think about the usage of non-Si materials to improve power electronics since on-resistance reduction is essential for heating and power loss issues [3]. Also, a movement away from using Si materials for power devices is due to Si's limitations. Silicon

$$R_{ONsp} = \frac{1.716 \times 10^{-6} \varepsilon_r{}^{0.5} V_B{}^{2.5} E_g{}^{-3}}{\mu_e} \quad \text{(Equation 1)}$$

has a relatively low breakdown field of .3 MV/cm compared to that of wide bandgap materials'. Beneficial properties of wide bandgap other than the lower on-resistance include large bonding energy which make it resistant to chemical attacks, high temperature resistance and large breakdown voltage [3]. Thus, research and study into wide bandgap materials is active.

Table 1: list of different semiconductor properties [3],[4],[5],[6],[31]

	Band Gap (eV)	Thermal Conductivity W/(cm• K)	Breakdown Field (MV/cm)	Mobility of electrons in devices (cm^2/(V• s) at 300K	Mobility of holes (cm^2/(V• s) at 300K
Ge	0.66	0.602	0.1	3900	1900
Si	1.12	1.49	0.3	1400	450
(Si)Ge	0.804-1.05	0.083-0.11	0.15-0.25	3900	1900
InP	1.344	.68	.5	5400	200
GaAs	1.4	0.55	0.4	8500	400
SiC	3.26	4.90	3	720	15-21

GaN	3.49	1.60	3.5	900	10

Even though materials such as SiGe, GaAs and InP have great mobility of either electrons or holes, they do not have as beneficial characteristics for power devices as wide bandgap semiconductors of SiC and GaN as seen in Table 1. GaN and SiC have more than five times the breakdown field of InP (3.5, 3 and 0.5 MV/cm respectively). Large breakdown fields allow a device to switch under large voltage and currents without device breakdown. Furthermore, wide bandgaps enable materials to be used in caustic and high temperature environments because they require more energy to create electron hole pairs thermally or caustically [7].

In the 1980s and early 1990s SiC was utilized for power devices due to many of the properties listed above. SiC devices were versatile to work in more extreme environments than Si, as SiC could operate at higher temperatures (150 ^{o}C – 175 ^{o}C and when properly packaged, >200 ^{o}C) than Si. With beneficial properties similar to those of Si as well, SiC has the ability to grow oxide layers thermally, thus making SiC MOSFET fabrication possible. The breakthrough of SiC MOSFETs resulted in a transistor with three desirable characteristics of power switching: high voltage, low on-resistance and fast switching speed [3]. A 900 V SiC MOSFET has approximately 35x smaller chip area than a 600 V - 900 V Si MOSFET, too. While SiC MOSFETs seem like the dominant technology in power switching, GaN has the potential to be the material for power switching transistors.

GaN has many superior properties compared to SiC. GaN has a 20 % higher breakdown field [7], and can be grown on different substrates (e.g. Si and sapphire) that are cheaper than SiC. Another advantage is that GaN's polarity effects allow it to have a high electron mobility transistor (HEMT) structure (more details on HEMTs are in Chapter 2). GaN HEMTs have a simpler and more cost effective fabrication process because there is no need for dopant insertion nor any need to grow a gate oxide for HEMTs [7]. To add, GaN devices have lower on-resistance based off the BFOM. This leads to lower power loss which in turn produces less heating in devices. The decrease in heating drastically reduces heat-sinking requirements [8] and allows for a decrease in amount/quality of cooling factors and increases the money saved. Furthermore, GaN's wide bandgap allows its devices to be used in caustic and high temperature environments (similar to SiC).

The current disadvantage of GaN is that there is a higher defect density of 108 cm2 when grown on SiC and a higher cost when grown on SiC [7]. High enough defect densities can cause leakage to occur in

high voltage situations. Another disadvantage of GaN HEMTs is that they are normally ON devices which is not desirable because we want our devices to be normally OFF when no voltage is applied [7].

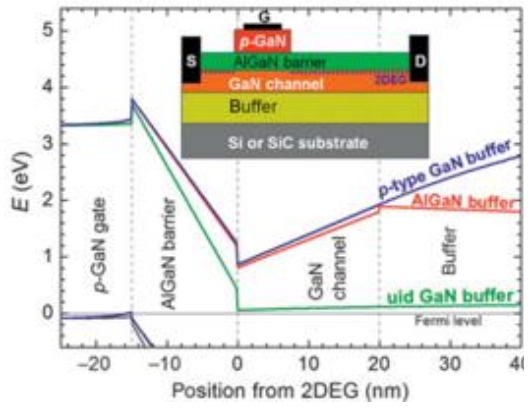

Figure 2: Band diagrams of a normally OFF HEMT utilizing p-GaN gate technology and different buffer materials [9]

For a transistor, having normally OFF characteristics is deemed to be the norm. To have a current flowing when no voltage is applied to the gate of a FET is considered unsafe [7]. Engineers do not want unnecessary power flowing when voltage is not applied. Since GaN HEMTs are normally ON devices, I want to look into ways of making these transistors normally OFF.

Some processes that have been done to achieve normally OFF characteristics are methods to thin out the 2-dimensional electron gas (2DEG). Some methods include thinning the AlGaN barrier beneath the gate [9]. Another method is to incorporate fluorine into the AlGaN layer beneath the gate to remove the 2DEG [9]. These methods do not work for power electronics because the result of these processes is a lowering of threshold voltage (Vth) below 1 V. There is also an observed 2 V gate swing and high ON gate current [9]. For power electronics, it is desired to have a larger Vth and gate swing due to the high power applications performed. To increase gate swing and decrease gate current, insulator layers can be added; however, the insulator deposition creates traps that deteriorate the device switching performance and make the HEMT less reliable [9].

Another school of thought to achieve normally OFF characteristics is to connect the drain of a standard Si MOSFET to the source of a GaN HEMT with its gate grounded in a cascade configuration [9]. However, this combined device cannot turn fully ON because that would require a positive gate bias for the HEMT. To add, the Si MOSFET will increase input capacitance and in turn increase switching losses [9].

A proposed technique presented by Oliver Hilt and other engineers of the Ferdinand Braun Institut was to use p-GaN gate technology along with an AlGaN or doped GaN buffer. P-type gates require the gate to contain Mg-doped GaN with a doped ohmic contact. This gate type provides an acceptable Vth of up to 4 V and gate swing [9]. More importantly, this gate causes normally OFF characteristics for HEMTs by depleting the 2DEG when no bias is applied [9]. This pGaN gate method causes the Fermi level to drop

below the conduction by almost 1 eV as shown in Figure 2 [9]. The 2DEG will form once positive voltage is applied above threshold.

Table 2: Breakdown Voltages of different buffer materials grown on a SiC substrate

Buffer Material	Breakdown Voltage Scaling
$Al_{0.05}Ga_{0.95}N$ on SiC	~40 V/µm
GaN: C on SiC	110V/µm
GaN: Fe on SiC	50-60 V/µm
GaN on Si	80-90 V/µm

The engineers of Ferdinand Braun Institut fabricated multiple p-GaN gate transistors with different buffer materials to determine which buffer obtained optimal results in terms of blocking voltage and lateral blocking [9]. The buffer materials used included carbon doped GaN (GaN:C), iron doped GaN (GaN:Fe) and an $Al_{0.05}Ga_{0.95}N$. The conclusion was that the GaN:C buffer provided the highest scaled breakdown voltage of 110 V/µm as observed in Table 2.

I am proposing to simulate a normally OFF GaN HEMT based on these ideas. The HEMT layers will consist of a Si (111) substrate, an AlN nucleation layer, 2 GaN:C buffer layers with differing layers of doping, a GaN:C channel with a 20 nm $Al_{0.25}Ga_{0.75}N$ barrier and a p-GaN gate as seen in Figure 2. I propose to produce a GaN HEMT with an equilibrium Fermi level under the conduction band.

2. Literature Review

The transistor structure for GaN is the high electron mobility transistor or the HEMT. Like a MOSFET, a HEMT has a source, drain and gate electrode. The difference between a HEMT and Si MOSFET, however, is that HEMTs have an $Al_xGa_{1-x}N$ barrier layer instead of an oxide and have a GaN layer instead of a Si p or n well. Also, HEMTs do not necessarily need Si substrates. GaN HEMTs are also transistors with strong power switching device properties: high breakdown voltage, high switching speeds, low ON resistance and cheaper fabrication processes than their wide bandgap power transistor competitors in the SiC MOSFETs [14]. However, what concerns engineers is how these devices are normally ON—these devices can generate current without voltage applied to the gate [9]. Many applications of GaN HEMTs require them to be normally OFF due to unwanted power loss when gate voltage is not applied [9].

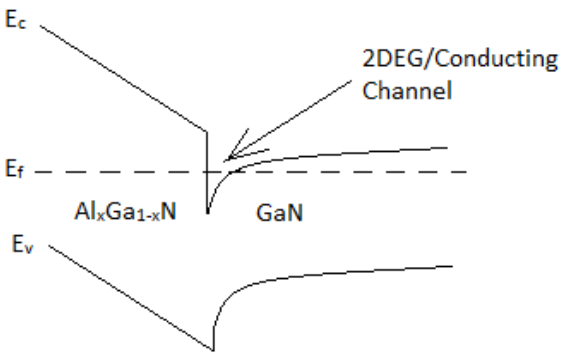

Figure 3: Energy band of the AlGaN/GaN heterostructure prevalent in normally ON HEMT devices

Looking into the source of the electron current of the normally ON device, it is a product of the naturally formed 2 dimensional electron gas (2DEG) in the transistor channel. The 2DEG is located where the Fermi level is above the conduction band near at the hetero-interface as seen in Figure 4. A collection of electrons are in the well that is confined by the AlGaN/GaN conduction band triangular quantum well and the Fermi level. The Fermi level is above the conduction at this interface due to the polarization effects of GaN.

Spontaneous polarization which occurs in III-V nitride devices is due to the non-symmetrical structure of wurtzite crystal around the central atom [12]. This results in a structural imbalance of positive and negative charge creating a dipole with the negative polarization vector pointing towards the nearest gallium atom from the nitrogen atoms. A HEMT with a Ga-polarity direction will have AlGaN bending down toward the substrate while an N-polar device will have the band bend upward toward the substrate [21]. Total polarization can be determined by adding up the individual spontaneous polarization values in each material which can be found in Table 1. Piezoelectric polarization also occurs at different material hetero-interfaces. The lattice mismatch causes strain induced polarization [17]. Tensile strain causes polarization in sync with spontaneous polarization and AlGaN/GaN structures display tensile strain in the AlGaN. This tensile strain makes the AlGaN energy band bend down toward

the GaN substrate if the structure displays Ga-Polarity [21]. The piezoelectric polarization can be calculated by the equation:

$$P_{PZ} = 2 \cdot \frac{a - a_0}{a_0}\left(e_{31} - e_{33} \cdot \frac{C_{13}}{C_{33}}\right) \quad \text{(Equation 2)}$$

where a and a_0 are lattice constants, e_{31} and e_{33} are piezoelectric coefficients and C_{13} and C_{33} are elastic constants. A full list of these values is in Table 3. The sheet charge caused by total polarization = $\sigma/(P_{PZ} + P_{SP})$ where σ is the surface charge density [20]. This spontaneous polarization in conjunction with piezoelectric polarization of the GaN/AlGaN interface is what creates the total polarization charges and fields of HEMTs and sets the Fermi level position in HEMTs [17].

Table 3: Polarity properties of different nitride materials [20]

Wurtzite	AlN	GaN	InN	BN
a_0(Å)	3.112	3.189	3.54	2.534[e]
c_0(Å)	4.982	5.185	5.705	4.191[e]
c_0/a_0	1.601	1.627	1.612	1.654[e]
	1.619[a]	1.634[a]	1.627[a]	⋯
u	0.380[a]	0.376[a]	0.377[a]	0.374[e]
P_{SP}(C/m^2)	−0.081[a]	−0.029[a]	−0.032[a]	⋯
e_{33} (C/m^2)	1.46[a]	0.73[a]	0.97[a]	⋯
	1.55[b]	1[c]	⋯	⋯
		0.65[d]	⋯	⋯
	1.29[e]	0.63[e]	⋯	−0.85[e]
e_{31} (C/m^2)	−0.60[a]	−0.49[a]	−0.57[a]	⋯
	−0.58[b]	−0.36[c]	⋯	⋯
		−0.33[d]	⋯	⋯
	−0.38[e]	−0.32[e]	⋯	0.27[e]
e_{15} (C/m^2)	−0.48[b]	−0.3[c]	⋯	⋯
		−0.33[d]	⋯	⋯
ϵ_{11}	9.0[b]	9.5[f]	⋯	⋯
ϵ_{33}	10.7[b]	10.4[f]	14.6[g]	⋯

To learn more about normally OFF HEMT characteristics, I looked into enhancement mode HEMTs, which are normally OFF devices with an isolated gate structure [12]. I researched four major enhancement mode techniques: gate recess, fluorine implantation, InGaN cap and p-GaN gate.

The ideology behind the gate recess method of enhancement HEMTs is to reduce the 2DEG at the interface by thinning the AlGaN barrier [13]. The process of growing these HEMTs is to grow the layers on an appropriate substrate (e.g. silicon) and then use RIE to etch down the AlGaN barrier to lessen its thickness to around 5 nm [12]. The etching is done in a plasma like BCl3 and then Ni/Au evaporated on top as contacts [13]. The result is a normally OFF device with Vth ≈ 0.4 V. The issue with this method is that RIE, being similar to dry etching, causes a relatively high density of defects in the device which can hurt current characteristics [9].

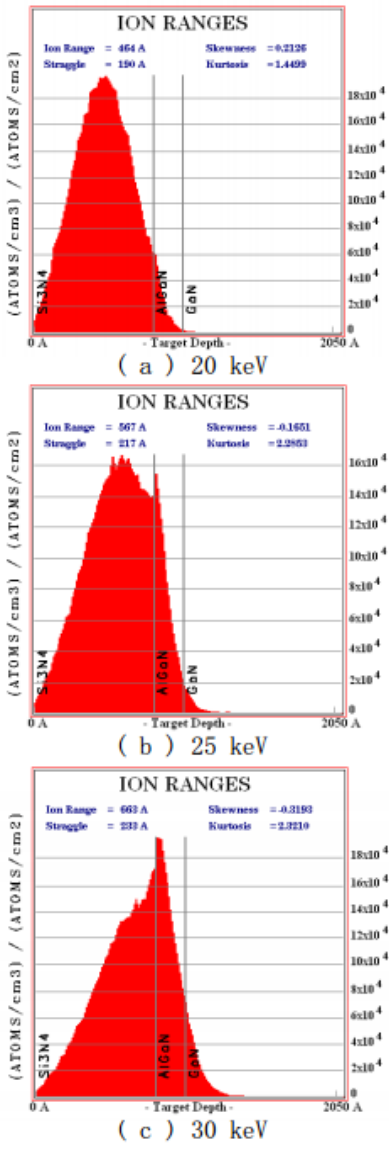

Figure 4: Doping profiles of F ion implantation in different GaN HEMT regions depending on implantation energy [15].

Another method is fluorine implantation, by which engineers lower the Fermi level of the transistor with the use of group 7 element fluorine. These fluorine ions insert negative charge within the AlGaN layer to lower its electric field and polarity [15]. These fluoride atoms are inputted into the AlGaN layer through high energy (25 eV) ion implantation [15]. Since the implantation doping profile has Gaussian shape with its edges having very small amounts of doping, to get more F ions in the AlGaN region, the implantation depth and energy need to be increased. However, the problem with deep implantation depth is having F ions implanted into the channel [15]. These impurities in the channel cause more scattering and a decrease in mobility. The optimized energy for implantation is 25 eV [15]. Doping energy profiles are shown in Figure 5. A way to have the ions not implant all the way into the channel is by growing an 80 nm Si_3Ni_4 layer atop the AlGaN to slow down the ion penetration. The resulting V_{th} is 0.6 V [15].

A third method of achieving an enhanced-mode HEMT is with the implementation of an InGaN cap layer. The introduction of a 5 nm InGaN layer [14] above AlGaN creates spontaneous piezoelectric polarization which opposes the polarization formed from the AlGaN/GaN layers. The band diagram of this structure has an upward sloping InGaN layer with a downward sloping AlGaN barrier layer next to it. These oppositely sloped layers display the difference in electric field sign and charge type at either the barrier/InGaN or the InGaN/AlGaN interface as shown in Table 4 (negative and positive charges respectively) [12]. The equation for polarization induced electrostatic charge density is:

$$\nabla \cdot P = \nabla \cdot \left(P_{sp} + P_{pz}\right) = -\rho_{pol} \qquad \text{(Equation 3)}$$

where P_{sp} is the spontaneous polarization charge density and P_{pz} is the piezoelectric polarization charge density cm^{-2} where P_{sp} and P_{pz} of the AlGaN/GaN point in the same direction--- the [0001] direction. However, with P_{pz} of InGaN/AlGaN points in the opposite direction. The opposing charges in turn raises the conduction band above the Fermi level leading to normally OFF characteristics which shifts V_{th} up by ~1.5 V compared to normally ON devices to a value of 0.4 V [14].

The last method I will introduce is the incorporation of a p-GaN gate. This idea is to have a GaN gate material which is highly p-type. The p-type doping is provided Mg being grown onto the gate in situ. In situ growth of a material takes place on another porous material, and in this case it is Mg on GaN. The p-type nature of the gate lowers the overall Fermi level all the way out to the substrate with Fermi level of 1 eV below the channel interface. What is beneficial about this p-GaN gate structure is that the resulting V_{th} is 4 V [9]. What is significant about this relatively larger threshold voltage is that it is more appropriate for power electronics usage [16]. For high power applications, it is more desirable to have larger V_{th} than 1 V [9]. This is why I will look into both the p-GaN technique of enhancement mode HEMTs and also into making V_{th} larger in other types of enhancement mode HEMTs.

Table 4: Interface charge density of GaN HEMT with an InGaN cap in cm^{-2}

Interface	D-mode	E-mode	Recessed E-mode
GaN/AlGaN	1×10^{13}	1×10^{13}	1×10^{13}
AlGaN/InGaN	–	-2.2×10^{13}	-2.2×10^{13}
InGaN/Passivation	–	1.4×10^{13}	–
AlGaN/Passivation	-0.6×10^{13}	–	-0.6×10^{13}

Table 5: Advantages and disadvantages of different Enhancement Mode techniques

Type of Enhancement Mode	**Advantages**	**Disadvantages**
Recessed Gate	Normally OFF	$V_{th} < 1V$, higher defect density
Fluorine Ion Implantation	Normally OFF	$V_{th} < 1V$, lowered mobility
InGaN Cap	Normally OFF	$V_{th} < 1V$
p-GaN Gate	Normally OFF; $V_{th} > 1V$	-----

To research the V_{th} characteristics of enhancement-mode HEMTs and normally OFF devices in general, I will need effective computational software to help me simulate certain device structures. The types of semiconductor simulation software provided by ICOR Lab are COMSOL, ANSYS and Sentaurus TCAD.

COMSOL is a simulation software that has a large bank of physical models such as "electrical" to "fluid mechanics." For electrical simulations, COMSOL indeed has a Semiconductor Module. COMSOL's Semiconductor Module is based on drift and diffusion equations with different thermal transport models. Looking into types of GaN HEMT simulations previously performed, I found no COMSOL simulations of enhancement mode GaN HEMTs. Most articles I read about COMSOL simulations addressed thermal characteristics of HEMTs. Other articles about COMSOL simulations and GaN were about optical devices such as LEDs and photodetectors.

ANSYS is another broad range simulation tool that has a multi-physics electronics and semiconductor package. Usage of ANSYS for GaN devices is present in Beijing University of Technology to determine thermal characteristics of HEMTs [19]. It does not stop at Beijing University; however, like COMSOL, most research I found that utilized ANSYS for GaN simulation were used for thermal characteristic modeling.

The last piece of simulation software provided by the University of Illinois is TCAD. TCAD, also known as Technology Computer Aided Design, is a simulation software that is tailored to semiconductors. TCAD can simulate both fabrication of devices and device behavior. TCAD has different device models that can prove useful for testing. TCAD device simulation works by using Newton's method of making better approximations using iterations [18] to solve Poisson's equation, continuity equations and other Maxwell's equations. These equations provide the necessary information to find out certain physics parameters of the device from electric field to hole current. Sentaurus TCAD has GaN piezoelectric polarization physics accounted for, too [18]. Another advantage of Sentaurus TCAD is that in its library of provided semiconductor devices, there is a HEMT structure. This will allow me to have a frame of reference when I try to model these transistors. Lastly, there are documented cases of simulated enhancement mode HEMT devices at Syracuse University and other institutions so I am confident that TCAD has the physical capability of modeling these devices so I can study their characteristics.

Table 6: The pros and cons of different simulation software

Software	Pros	Cons
COMSOL	Can model GaN HEMTs	Not as widely documented in usage as other software in terms of HEMT simulation
ANSYS	Can model GaN HEMTs	Not as widely documented in usage as other software in terms of HEMT simulation

TCAD	Specifically made for semiconductor simulation, many documented usages for GaN HEMTs (even enhancement mode HEMTs)	Large learning curve

3. TCAD Sentaurus Introductory Information and Simulations

TCAD Sentaurus has a steep learning curve and to prepare for more advanced simulations the basics of the software must be understood. To begin, one needs to be familiar with the 3 types of files needed for simulation: the parameter file, device structure file and the simulation script.

The parameter file contains material parameters. These parameters such as mobility, strain constants, and lattice constants can be edited and defined by the user; however, there are also default TCAD given parameter files with default values as well. To access parameter files for different files, in the command line we can type: "sdevice –P: GaN" or "sdevice –P: SiC" for example. Looking into the GaN parameter file, the parameters include permittivity of material in a vacuum, band structure parameters, piezoelectric coefficients and more.

The simulation script allows the user to perform certain measurements on devices. Parameters of measurement can include doping concentration, electron quasi-Fermi energy and electron mobility for example. Also, the simulation script allows the user to input what physics they want to incorporate in the simulation such as mobility being a function of doping dependence. A list of different physics can be found in the simulation manual. We also declare what DC voltage ramp we want to put on the contacts and how many iterations we want per Newton's method build condition.

The device structure file is where the user scripts their own devices. To make a complex device structure file, a vast amount of knowledge is needed (over 1800 pages of informative content is provided in the structure file manual that Synopsis provides for TCAD Sentaurus).

When I first started TCAD simulation, I started with the most basic structure I could: a rectangular slab or silicon. I expanded my comfort level by adjusting the doping of the slab and eventually made a rectangular PN junction diode and ran simulations on it. For a PN junction, there has a gradient of mesh points which are very fine near the junction but can be coarse around the bulk materials.

In addition my first basic TCAD device structure was 10 µm in length with the acceptor and donor doping levels of 1×10^{18} cm^{-3} for both boron and phosphorus. I started off by measuring the built-in electric field based on Eq 4 to see if it corresponded to the theoretical value.

$$|\mathcal{E}(x)| = \begin{cases} \frac{qN_a}{\varepsilon_s}(-x - x_p);\ -x_p < x < 0 \\ \frac{qN_d}{\varepsilon_s}(x - x_n);\ 0 < x < x_n \end{cases} \quad \text{(Equation 4)}$$

The max electric field magnitude was $|E(x)| = \frac{qNa}{\varepsilon s}(x_p)$ if the diode's junction was centered about x = 0.

To find X_p we had to find the depletion width, which is dependent on built-in voltage

$$x_d = \sqrt{\frac{2\epsilon_s}{q}\phi_{bi}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)} \qquad \text{(Equation 5)}$$

$$\phi_{bi} = \frac{kT}{q}\left(\frac{N_a N_d}{{n_i}^2}\right) \qquad \text{(Equation 6)}$$

where $\phi_{bi} = 0.935\ V$. Thus X_d = 0.049 µm, x_d = 0.5, X_p = .0245 µm and $|E(x)|_{max}$= 379, 227.614 V/cm.

The first time I compiled my design and plotted the E field, I had the plot shown on the left of Figure 5. $|E(x)|_{max}$ was around 2.25E5 V/cm which is more than 1E5 V/cm less than the theoretical value. I determined that since the depletion region was around 0.05 µm, and my current minimum mesh size was .01 µm near the junction, there were around 5 mesh locations having calculations. To increase the amount of computation around the junction, I decreased the mesh size by a factor of 10 so there would

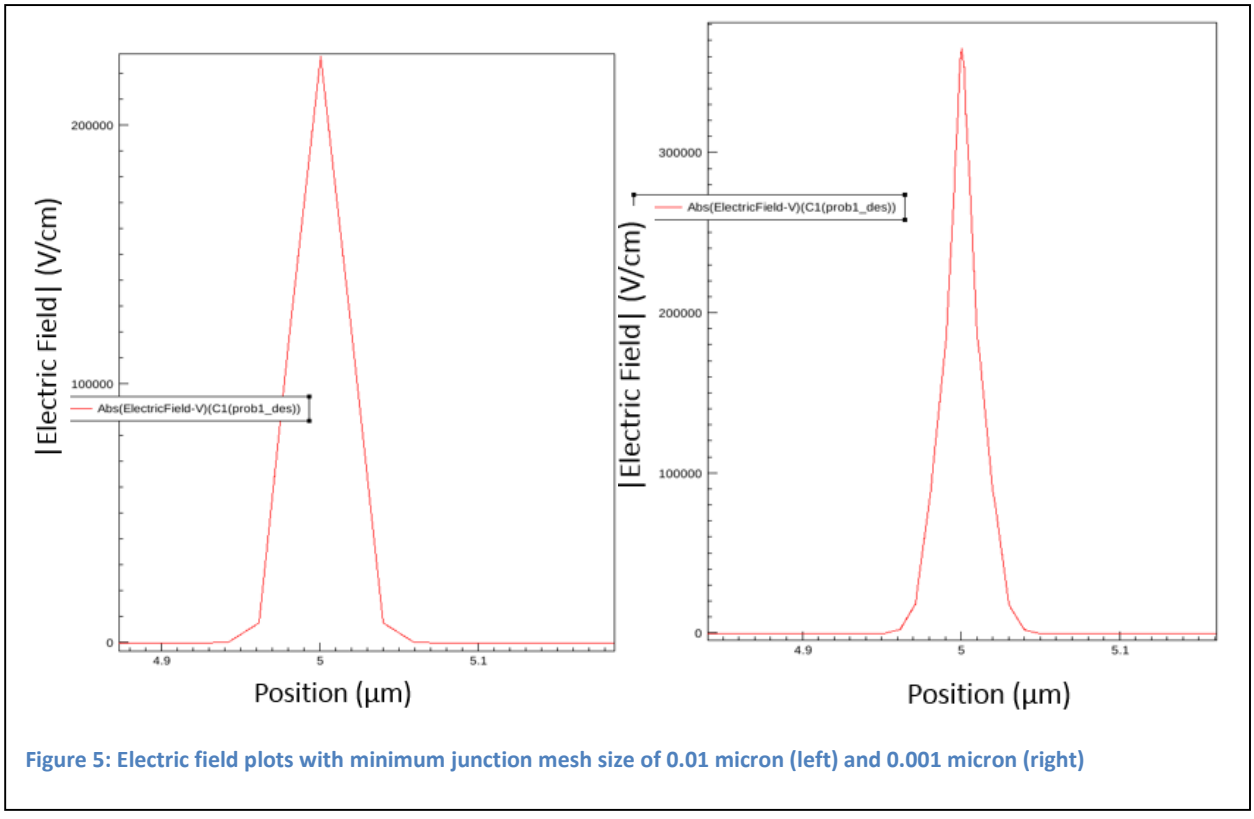

Figure 5: Electric field plots with minimum junction mesh size of 0.01 micron (left) and 0.001 micron (right)

be 50 points of sampling within the depletion region. The corresponding E field curve (Figure 5 right plot) shows a more theoretical $|E(x)|_{max}$ of around 3.7 E5 V/cm.

Next, I plotted the potential profile across the diode. The resulting built-in potential was around .9 V which corresponds to the theoretical value calculated as seen in Figure 6.

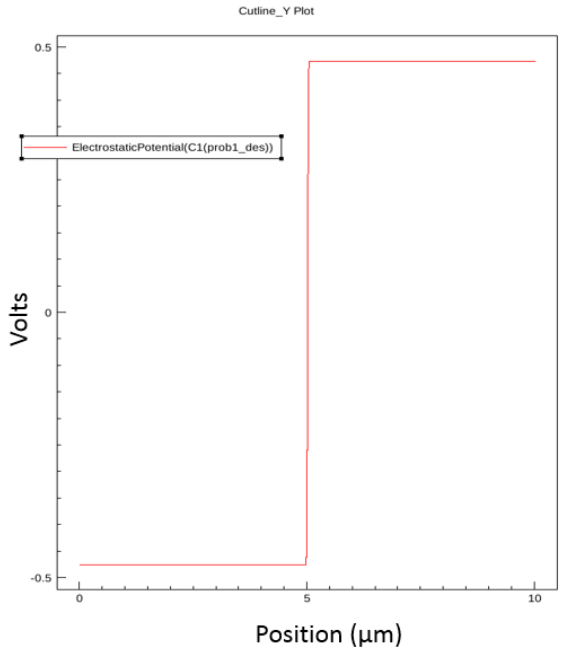

Figure 6: Potential profile of PN junction (voltage vs position)

Lastly, I looked into the IV characteristics of this diode to see if they matched the curves of realistic diodes. The forward biased curve of the diode is exponential.

When I observed the reverse-bias voltage in my simulation script, I was curious to see if TCAD can model reverse bias breakdown effects. I had the physics in my simulation script to include avalanche and Shockley-Read-Hall recombination, so in theory, the diode would break down with impact ionization. The device showed that it indeed had a relatively large negative current at high reverse bias and then no current at even larger negative current.

As I have successfully simulated a PN junction diode, HEMTs are entirely different structurally. I will use what I have learned in this basic simulation with provided transistor template files from the TCAD library to create a GaN HEMT. I will edit these provided files to help me replicate HEMT structure files and manipulate the different regions to have optimal doping values, mesh thickness, and material thickness.

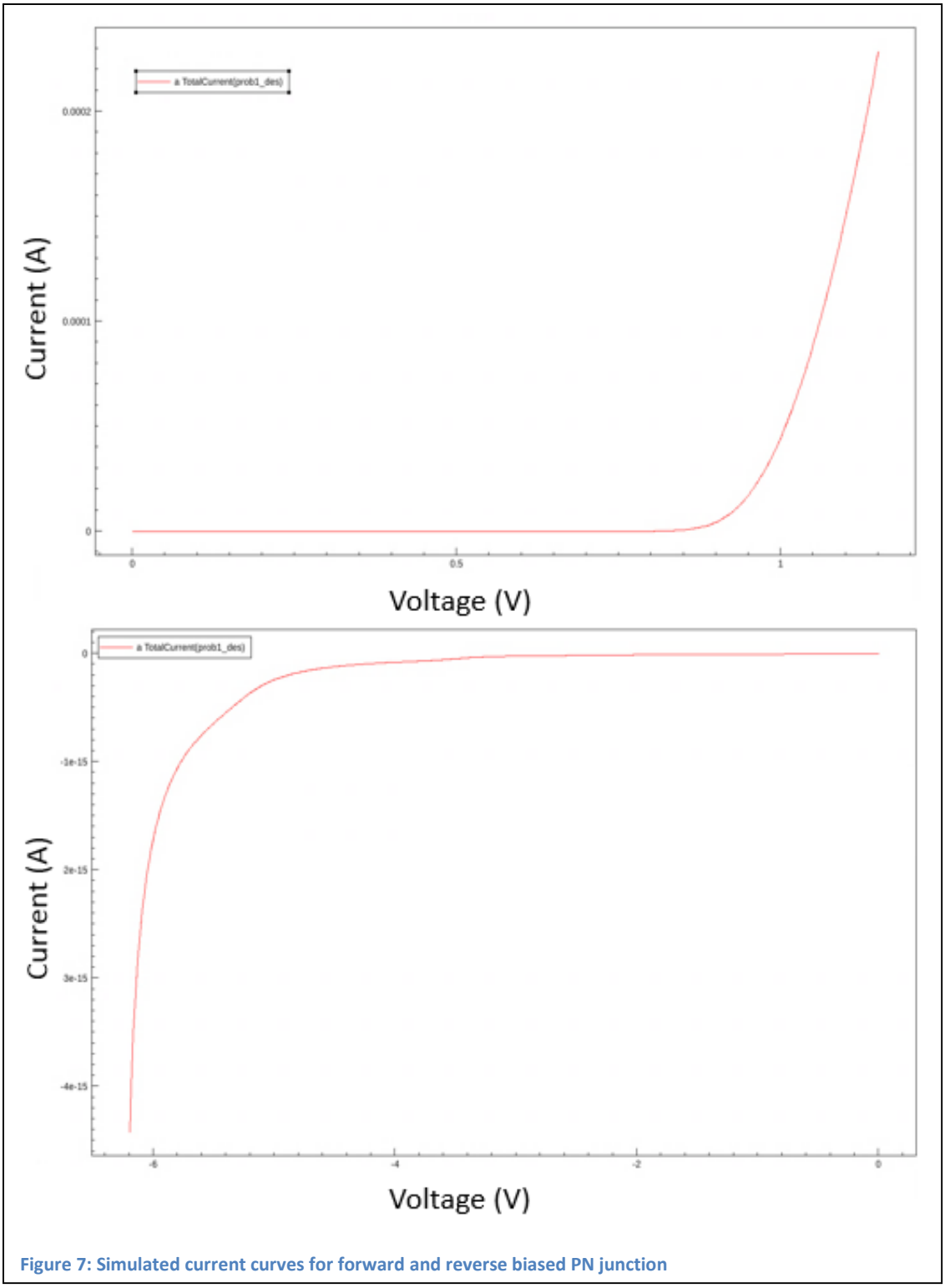

Figure 7: Simulated current curves for forward and reverse biased PN junction

4. Normally OFF pGaN HEMT TCAD Simulations

My plan of attack of simulating enhancement mode HEMTs has three parts. The first part is to understand the three TCAD simulation files: structure, simulation and parameter files. The second is to look into the library of provided files given to the users of Sentaurus TCAD of more advanced devices to try and understand the structures of similar transistors while comparing and contrasting them to the structures of p-GaN enhancement mode HEMTS. The third is to look at different research papers of p-GAN HEMTs and see if it is possible to reproduce the structure, simulation conditions and material parameters in the TCAD software.

The file/structure in TCAD's given library I used for my reference was called GaN HFET. This structure consisted of layers: SiN passivation, GaN cap, $Al_{0.25}Ga_{0.75}N$ barrier, GaN layer and SiC substrate. The thickness of each layer is given in Table 7 while the structure is seen in Figure 9.

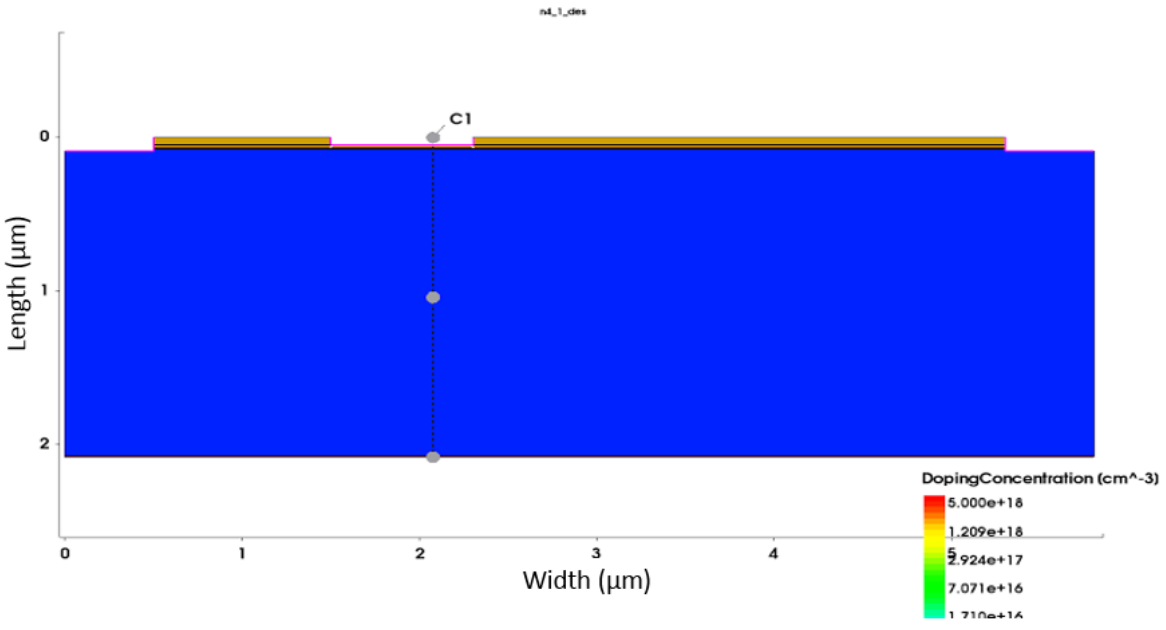

Figure 8: Provided GaN HFET structure given by TCAD Sentaurus

Table 7: Thickness of each GaN HFET layer

Layers from top to bottom	Thickness of each layer
SiN passivation	0.05
GaN Cap	.003 µm
AlGaN	.02 µm
GaN	2 µm
SiC substrate	0.01 µm

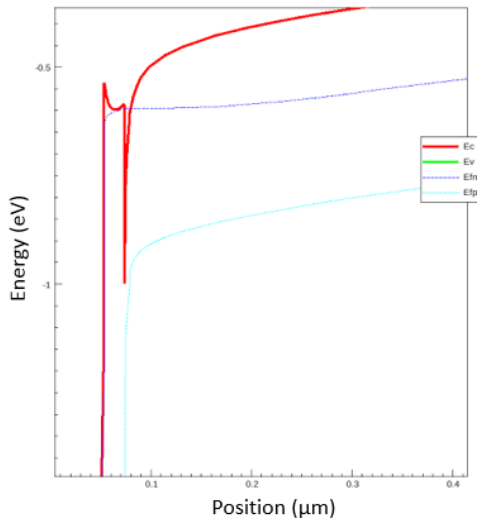

Figure 9: Corresponding conduction band plot around the provided GaN HFET interface

To confirm the physics of the GaN HFET, I looked into its band structure, mobility vs. position and electron concentration vs. position around the $Al_{0.25}Ga_{0.75}N$/GaN interface to see if there was evidence of a 2DEG layer. As seen in Figure 10, the conduction band of the device shows that at the hetero-interface, the Fermi level is above the conduction band. Also, the electron mobility vs. position graph had a positive spike in electron mobility near this interface, confirming the high mobility electrons in the 2DEG.

The GaN HFET was has a normally ON HEMT structure that is structurally sufficient for me to use as a reference to create a normally OFF pGaN HEMT. The enhancement mode HEMT I plan to recreate is Liang-Yu Su's p-GaN gate [22] with parameters and structure shown in Table 8 and Figure 11 respectively.

Table 8: Thickness of each of Su's p-GaN gate HEMT layer

Layers from top to bottom	Thickness of each layer
p-GaN cap	.06 µm
$Al_{0.25}Ga_{0.75}N$ barrier	.01 µm
GaN (intrinsic)	1.2 µm
Si substrate and buffer(AlN and Si)	2.4 µm

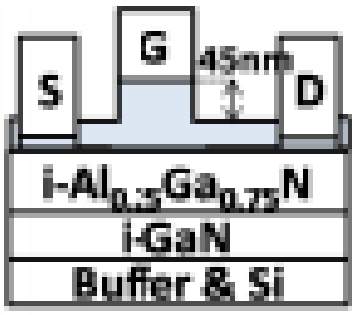

Figure 10: Su's enhancement mode HEMT structure

It took plenty of trial and error to troubleshoot the problems I encountered such as errors in script and dimension mismatch, but the end result was a successfully created semiconductor device as seen in Figure 11.

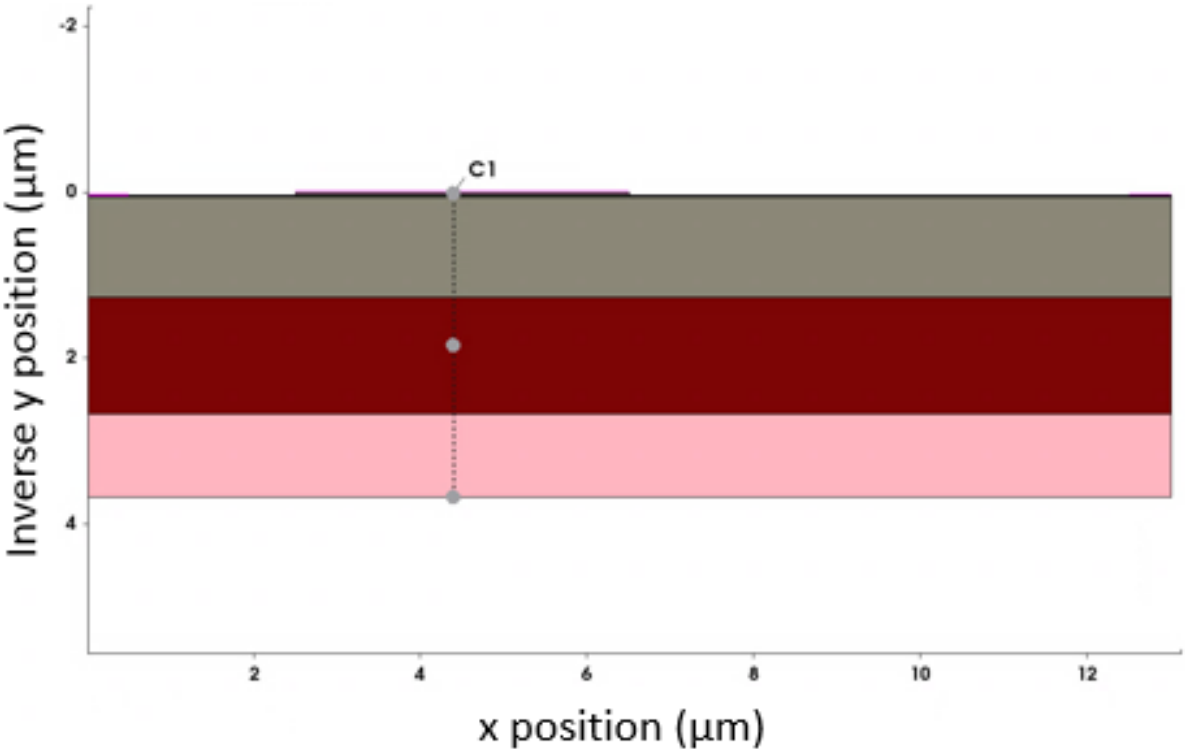

Figure 11: My created rendition of Su's p-GaN gate enhancement mode HEMT

Su's paper was unclear on the material for the buffer layer, so I created an AlN nucleation layer as done in the provided TCAD HFET file. This nucleation layer appears relatively thick compared to the GaN and substrate layers and I will need to research more on HEMT buffer layers and the material stacks they are comprised of, but for now the band diagram seems to produce normally OFF graphs as can be seen in Figure 11.

Another deviation from Su's p-GaN structure is that he used magnesium doping as the p-type dopant of the p-gate but TCAD Sentaurus did not recognize the magnesium doping so I browsed their dopant list and decided to use generic "AcceptorActiveConcentration" to generate p-type doping. The result is having the conduction band above the Fermi level by around 1 eV, rendering it normally OFF. I also simulated this device with no p-doped GaN gate to see the difference in bandgap structures. The simulated device with no p-type doping had a normally ON band structure. The comparisons of the two graphs can be seen in Figure 12.

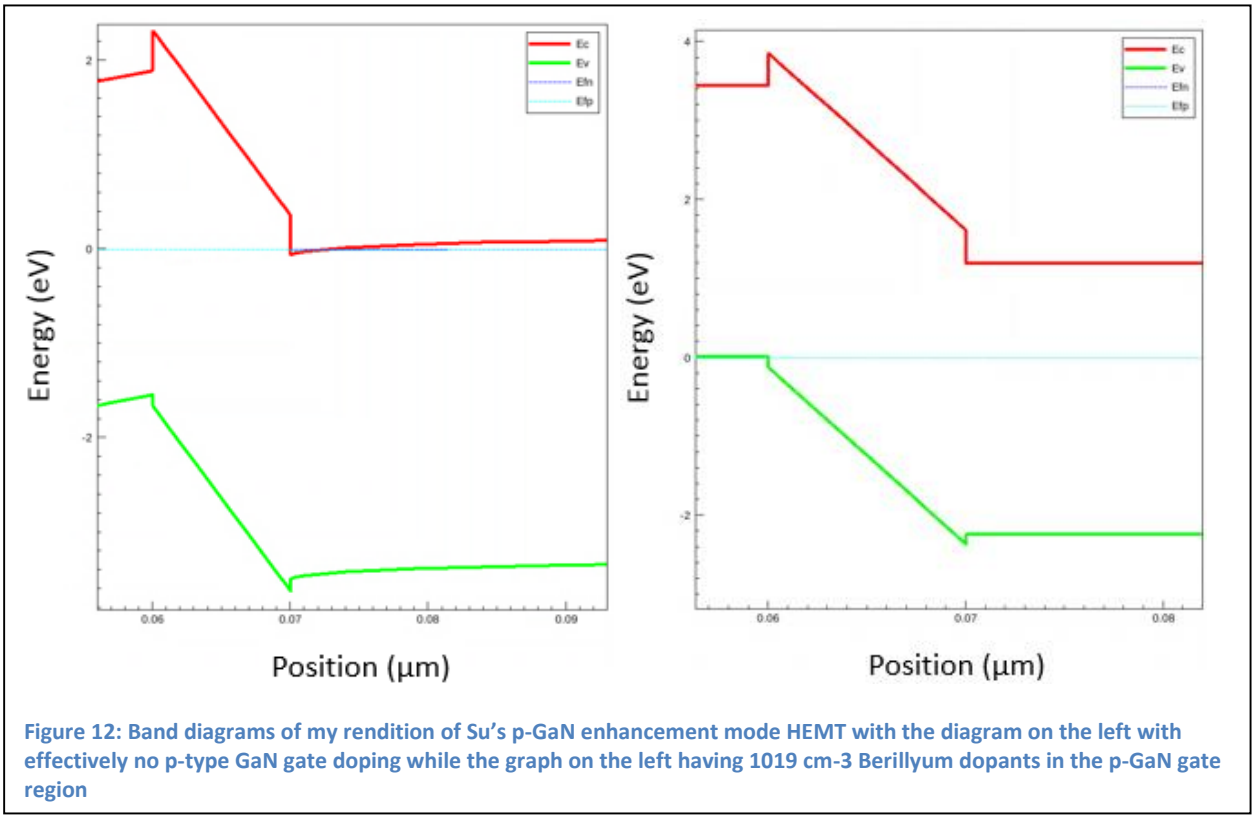

Figure 12: Band diagrams of my rendition of Su's p-GaN enhancement mode HEMT with the diagram on the left with effectively no p-type GaN gate doping while the graph on the left having 1019 cm-3 Berillyum dopants in the p-GaN gate region

The next step is to analyze the IV characteristics of the created enhancement mode HEMT to determine if the parameter physics and structure are correct. My first few runs, I struggled with simulating IV curves for the pGaN HEMT. The referenced device (GaN HFET) file's simulation script gave me a logarithmic MOSFET IV curve when I had set the gate voltage to no bias with V_{ds} ramped to 6 V as seen in Figure 14. The current rises and saturates around 3 V with the magnitude of current being along the order of 10^{-6} A as seen in Figure 13. This is a fairly reasonable range for an OFF state current with a bit of leakage. However, there were convergence issues when I simulated curves with gate voltages above 0.5 V.

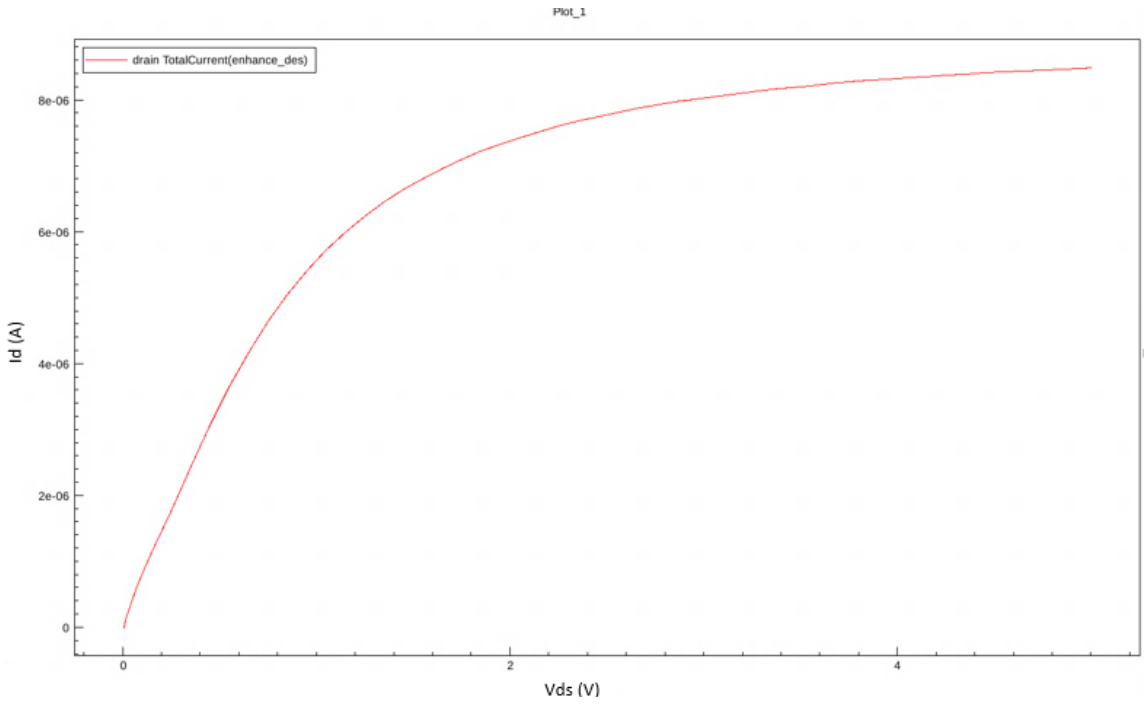

Figure 13: IV Curve of created HEMT with Vg = 0

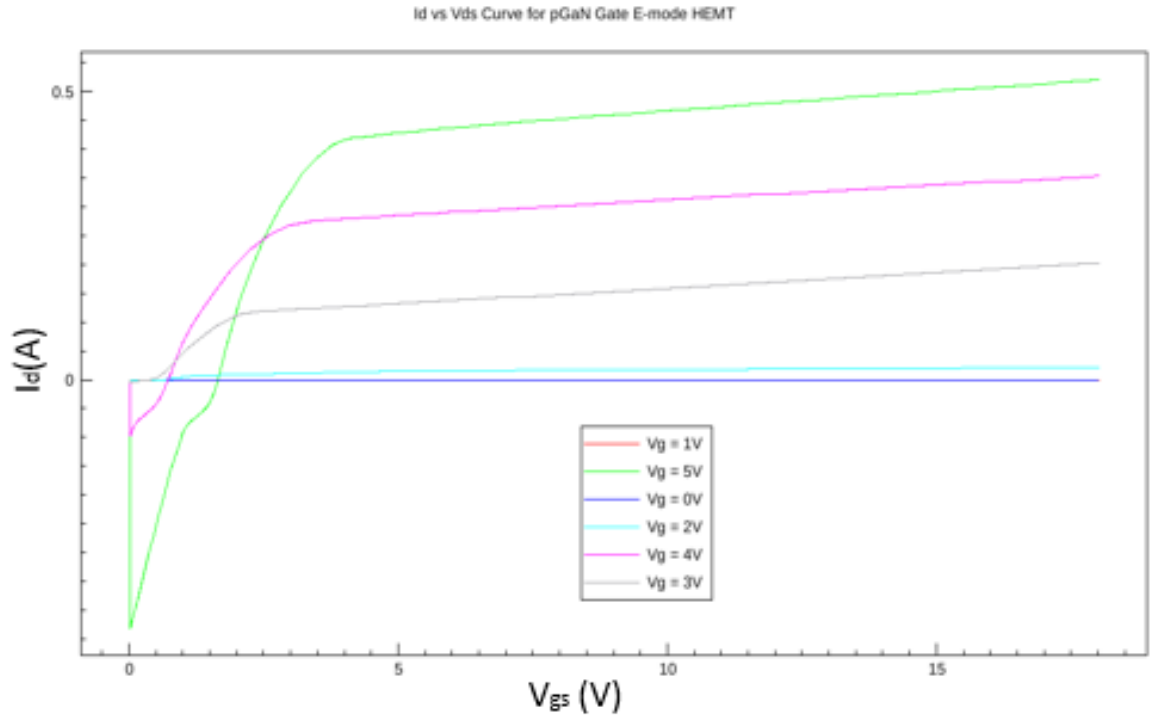

Figure 14: Simulated IV curves for the pGaN HEMT with "Power Devices" parameters and simulation script

Having convergence issues with the GaN HFET simulation script, I looked into what other devices were

provided to us in TCAD Sentaurus. I found a folder called “Power Devices” and traversing through this list, I found GaN HEMTs in this file. Using their provided simulation script and parameter file for the power device on my created structure, there were no more convergence issues with higher gate voltages. The first few simulations with the new simulation script and parameter file had IV curves produced with gate voltage ranging all the way up to 6 V. I was convinced that this GaN power transistor provided script was adequate for the type of device I created. The resulting IV curves I got are displayed in Figure 14. The IV curves have similarities to ideal transistor IV curves but also diverge from them. The drain current increases per drain voltage as the gate voltage is biased more. However, for higher gate voltages, there is negative drain voltage for V_{ds} values lower than 2 V. I believed that there could be a physical parameter issue with my device or simulation script. I reevaluated my simulation parameter file and compiled the list of parameter equations for GaN, the given values for different constants. I cross checked these constants against research papers to find confirmed values of each parameter. The results are given in Appendix A.

Along with these parameter updates, I also had the voltage range for the gate bias go up to only 3 V instead of 5V as there seems to be leakage with gate voltage above 3 V. The resulting I_d vs. V_{ds} curve is more transistor-like with minimal leakage. The turn-on voltage for the new transistor curve is seen to be above 1.5 V as seen in Figure 15. To clearly discern what the turn on voltage of the device is, I went and examined the I_d vs V_{gs} IV curve to determine at what gate voltage the HEMT would conduct electricity. The result is also in Figure 15 with a V_t of around 1.8 V. This is in the range of power device turn-on voltage.

While the created pGaN HEMT has MOSFET-like characteristics and IV curves, this created device has some limitations. As seen in my previous simulations, when the gave voltage is above 3 V, the device displays negative leakage current which is possibly due to breakdown in the pGaN material. Also, while MOSFET IV curves have saturation currents with a positively increasing slope, HEMTs have a theoretical downward sloping I_d curve after a certain V_{ds}. This suggests that even though my simulated HEMT IV curve is accurate for a MOSFET, it may not be completely accurate for a HEMT device. I believe that I may be simulating the naturally occurring trap states of HEMT devices incorrectly. However, I believe that the simulation results are valid enough for me to assume that with the addition of a pGaN gate

layer atop of the AlGaN barrier layer for a GaN HEMT, the GaN HEMT will become a normally OFF device with a voltage range around 1-2 V.

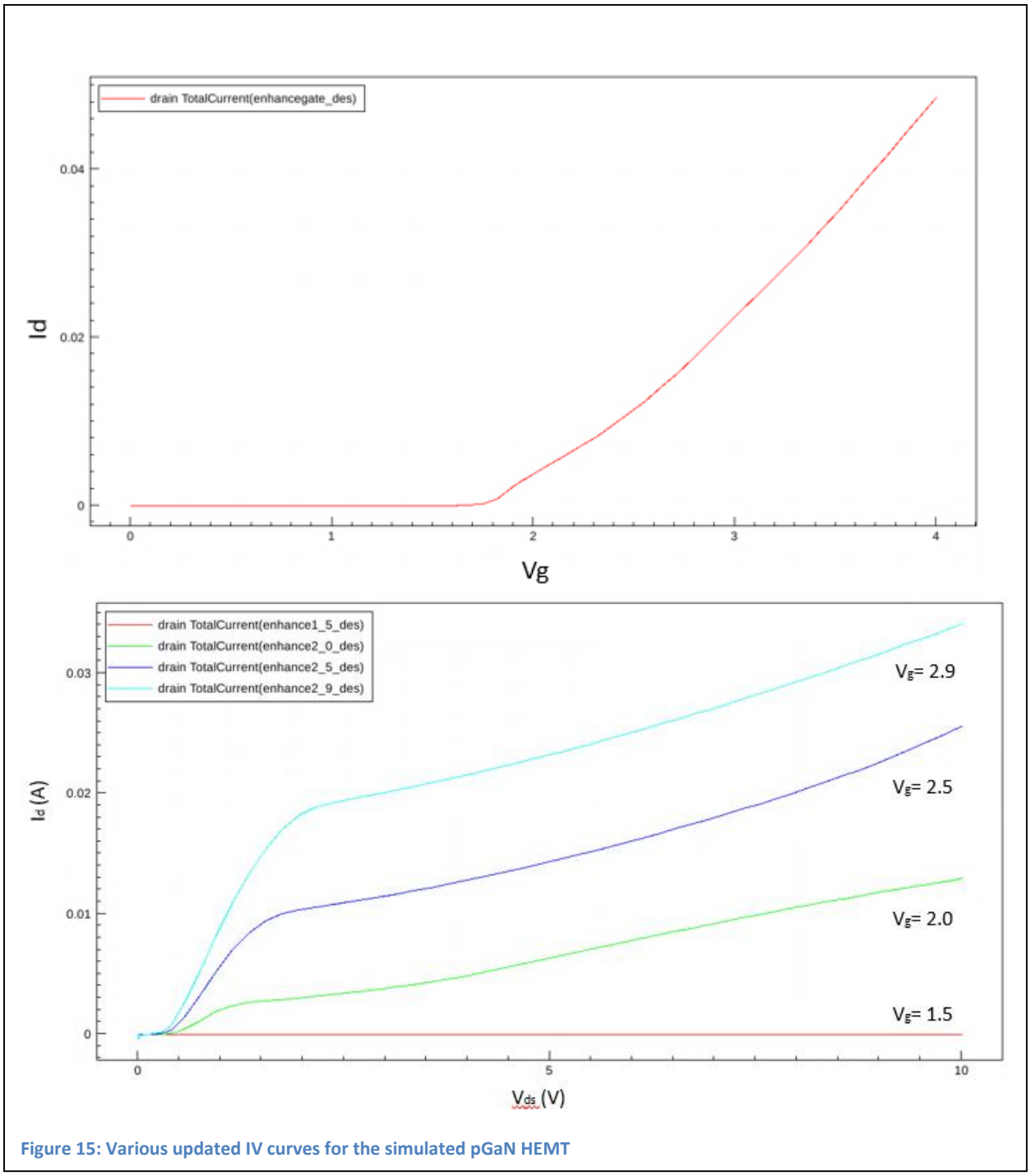

Figure 15: Various updated IV curves for the simulated pGaN HEMT

5. Conclusion

Gallium nitride has many beneficial properties for transistor usages beyond the limitations of silicon. Its large breakdown electric field and wide bandgap make ideal in power switching devices. However, the inherent flaw of the GaN HEMT in terms of power devices is the HEMT's naturally conducting electron channel. Producing normally OFF HEMTs is essential for safety and to reduce power leakage issues in these devices. There are many methods of achieving enhancement mode, but the pGaN gate method is the most effective. With its high V_{th}, it is ideal to put a p-doped GaN layer below the metal gate. Using Synopsys TCAD to simulate a pGaN gate HEMT can help us confirm the effectiveness of this enhancement mode method. The results are that the device is a normally OFF one with a threshold voltage of around 1.8 V. The gate voltage range, however, is limited to below 3V as we see leakage current at voltages above 3 V possibly coming from pGaN breakdown. With this result, we can effectively create GaN power devices but still need to be wary of leakage at very high gate voltages.

Appendix A: GaN TCAD Simulation Parameters

Table 9: TCAD Simulation Parameters

Equation	Values	Ref
Lattice Parameters:	X = (1, 0, 0) Y = (0, 0,-1)	[18]
Piezoelectric Polarization: $P_{PZ} = 2 \cdot \frac{a - a_0}{a_0}\left(e_{31} - e_{33} \cdot \frac{C_{13}}{C_{33}}\right)$ (Equation 7) Where the Relaxation Constant value is: $\left(e_{31} - e_{33} \cdot \frac{C_{13}}{C_{33}}\right)$ (Equation 8)	Relaxation: 0.24 ****changed from 0.2 A_0 = 3.185 angstroms	[12]
Dielectric constant: ϵ	9.5 (isotropic) ****changed from 9.4 10.04 (anisotropic)	[23]
Bandgap: $E_g(T) = E_g(0) - \left(\frac{\alpha T^2}{T + \beta}\right)$ (Equation 9)	$E_g(0)$ = 3.40 [eV] ****changed from 3.507 [eV] α = 9.09 E -4 [eV/K] T = temperature [K] β = 800 [K] ****changed from 836 [K]	[24] [25]
Effective Temperature Dependence Density of States for Valence Band: $N_v(T) = N_v(300)\left(\frac{T_p}{300}\right)^{\frac{3}{2}}$ (Equation 10)	$N_v(300\ K)$ = 4.6 E 19 [cm^{-3}] ****changed from 2.5 E 19 T_p = temperature [K]	[26] [27]
Effective Temperature Dependence Density of States for Conduction Band: $N_c(T) = N_c(300)\left(\frac{T_n}{300}\right)^{\frac{3}{2}}$ (Equation 11)	$N_c(300\ K)$ = 2.30 E 18 [cm^{-3}] ****changed from 2.65 E 18 T_n = temperature [K]	[26] [27]
Effective Mass for Holes: $\frac{m_p}{m_0} = \left(\frac{N_V(300)}{2.540 \times 10^{19}}\right)^{\frac{2}{3}}$ (Equation 12)	$N_c(300\ K)$ = 2.30 E 18 [cm^{-3}] ****changed from 2.65 E 18	[26] [27]
Effective Mass for Electrons: $\frac{m_n}{m_0} = \left(\frac{N_C(300)}{2.540 \times 10^{19}}\right)^{\frac{2}{3}}$ (Equation 13)	$N_c(300\ K)$ = 2.30 E 18 [cm^{-3}] ****changed from 2.65 E 18	[26] [27]

Table 10 Continued			
Mobility Model: $\mu_L = \mu_L^{300}\left(\frac{T}{300}\right)^{-\gamma}$ (Equation 14) *based off mobility of Si inversion layers		(electron value, hole value) γ = 1.5, ****changed from 1, 2.1 μ_L^{300}= 1600, _____ [cm^2/Vs] ****changed from 300, 14 [cm^2/Vs] T = temperature [K] T_0 = initial temperature [K]	[28] [29]
Doping Dependent Mobility Model: $\mu_{dop} = \mu_{min1}e^{-\frac{P_c}{N}} + \frac{\mu_{const} - \mu_{min2}}{\left(1+\frac{N}{C_r}\right)^{\alpha}} - \frac{\mu_1}{\left(1+\frac{C_s}{N}\right)^{\beta}}$ (Equation 15) *Based off a mobility model that is tailored to Si		(electron value, hole value) μ_{min1} = 85, 33 [cm^2/Vs] μ_{min2} = 75, 0 [cm^2/Vs] μ_1 = 50, 20 [cm^2/Vs] P_c = 6.5 E 15, 5.0 E 15 [cm^{-3}] C_r = 9.5 E 16, 8.0 E 16 [cm^{-3}] C_s = 7.2 E 19, 8.0 E 20 [cm^{-3}] α = 0.55, 0.55 β= 0.75, 0.7 N = total concentration of holes or electrons [cm^{-3}]	[30]
High Field Dependence (Caughey-Thomas model): $\mu_{n,p}(E) = \mu_{n0,p0}\left[1+\left(\frac{\mu_{n,p0}E}{v^{n,p}{}_{sat}}\right)^{\beta_{n,p}}\right]^{-1/\beta_{n,p}}$ (Equation 16)		$\beta_{n,p} = \beta_{0\,n,p}\left(\frac{T}{T_0}\right)^{exp}$ Where: • $\beta_{0\,n,p}$ = 1.7, 1.7 • exp = 0.0, 0.0 $V_{sat} = v_{A,sat} + v_{B,sat}\left(\frac{T}{T_0}\right)$ Where : • $v_{A,sat}$ = 3.0 E 7, 1.0 E 7 [cm/s] ****changed from 1.8 E7, 1.0 E 7 [cm/s] • $v_{B,sat}$ = 0, 0 [cm/s] • $V_{sat(min)}$ = 5.0 E5, 5.0 E5 [cm/s]	[29]
Recombination/Generation Models (Scharfetter): $\tau_v(N,T_L) = \tau_v{}^{min} + \frac{\tau_v{}^{max}(T_L) - \tau_v{}^{min}}{1+\left(\frac{N_D+N_A}{N_v{}^{SRH}}\right)^{\gamma_v{}^{SRH}}}$ (Equation 17) With: $\tau_v{}^{max}(T_L) = \tau_{v,300}\cdot\left(\frac{T_L}{300}\right)^{\alpha_v{}^{SRH}}$ (Equation 18) Where v = n,p		$\tau_v{}^{min}$ = 0, 0 [s] $\tau_v{}^{max}$ = 1.0 E -11, 1.0 E -11 [s] $N_v{}^{SRH}$ = 1 E 16, 1 E 16 [cm^{-3}] $\gamma_v{}^{SRH}$ = 1, 1 $\alpha_v{}^{SRH}$ = -1.5, -1.5	[12]

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