

# OPTIMIZATION OF OFF-STATE BREAKDOWN VOLTAGE IN GAN HIGH ELECTRON MOBILITY TRANSISTORS

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By

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## Abstract

Gallium Nitride (GaN) technology is the next revolution in electronics as it offers a large bandgap (high critical electric field) and high electron mobility (2D electron gas) in one transistor design, surpassing silicon (Si), gallium arsenide (GaAs), and indium phosphide (InP) based technologies. High efficiency and high voltage operation of GaN high electron mobility transistors (HEMTs) provide significant performance and size advantages over the aforementioned devices. GaN HEMTs are normally-on devices, meaning that the devices do not shut down even though no gate voltage is applied, due to the 2D electron gas channel. In applications where safety and efficiency are in the forefront, normally-off devices are preferred. A simple way to obtain a normally-off GaN HEMT is to apply a negative gate voltage. A challenge of normally-off GaN HEMT is that the devices usually fail before the critical electric field is reached. Breakdown is caused by gate-leakage impact-ionization, drain-to-source punch-through and vertical current leakage. Increasing the breakdown voltage would eliminate the damage in high voltage, high current applications and would extend the lifetime and operating bias conditions. The goal of this research is to design and simulate GaN-based power transistors in order to understand their different characteristics, such as voltage-current relations, using TCAD Sentaurus software. GaN HEMTs with different design strategies (i.e. doping concentration, layer thicknesses, layer contents) are simulated in order to understand their impact on off-state breakdown voltages. Based on the simulation results, different strategies to improve the off-state breakdown voltage are proposed.

Subject Keywords: Gallium nitride; High Electron Mobility Transistors (HEMTs); Breakdown voltage; TCAD Sentaurus.

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## Table of Contents

1	Introduction .....	1
2	Literature Review .....	3
2.1	Physics and Technology of HEMTs .....	3
2.2	Advantages of GaN based transistors .....	5
2.3	Bottlenecks of GaN HEMT Technology .....	8
2.4	Solutions for Bottlenecks of GaN HEMT technology .....	10
3	Description of Research Results.....	12
3.1	Research Goals Overview .....	12
3.2	Work and Contributions.....	13
3.2.1	Simulation of a P-N Junction.....	13
3.2.2	Simulation of GaN based Heterojunction FET (HFET) .....	21
3.2.3	Simulation of a GaN Power Transistor .....	27
4	Conclusion .....	37
	References.....	38

## 1 Introduction

One can consider the transistor as being the most important invention of the 20<sup>th</sup> century. The transistor, a solid state electronic device with three or more terminals connected to electric circuits, is the building block of all modern electronic devices. Before the first transistor was invented in 1947 at Bell Laboratories by John Bardeen and Walter Brattain, vacuum-tubes, invented in 1907, were used for radio technology amplification and long-distance telephony [12]. However, the vacuum-tubes had a very fragile aspect and consumed a lot of power. After the first transistor was invented, the transistor technology developed and made its appearance on the market very quickly. The first transistor was 10 cm long, but today 820 million transistors can be found on a 45 nm Penryn chip from Intel. Moreover, today, the number of transistors is higher than the number of grains of sand on Earth.

Since 1960, silicon has been the most commonly used semiconductor for transistor fabrication, due to its abundance on Earth. In 1965, Gordon Moore, co-founder of Intel Corporation, introduced “Moore’s Law” which stated that the number of transistors on chip will double every two years. After fifty years, scientists believe that Moore’s law might have come to a natural end. The smallest transistor today was invented in 2012 and is a single-atom transistor. Nowadays, researchers concentrate their work more on how to reduce the number of transistors used in a circuit instead of reducing the size of the transistor. Therefore, gallium nitride (GaN), a wide bandgap semiconductor, has become competitive against silicon in transistor fabrication.

We are essentially interested in GaN-based High Electron Mobility Transistors (HEMTs) used in power applications. GaN based HEMTs have five essential qualities which surpass

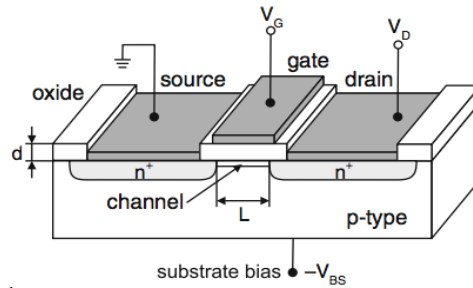
silicon (Si) based transistors [2]. First, GaN-based transistors have a lower on-resistance, which means lower conduction losses in the circuit. Secondly, we can have faster devices using GaN and so experience less switching losses when we use HEMTs in heart switching applications such as buck converters. Thirdly, the lower capacitance of GaN devices decreases the loss in charging and discharging the device. Also less power is required from the driver circuit. Moreover, the use of GaN lets us fabricate smaller devices which cover less space on the printed circuit board [2].

## 2 Literature Review

### 2.1 Physics and Technology of HEMTs

As we have introduced the notion of HEMTs, we should define the physics and functioning of the latter as well.

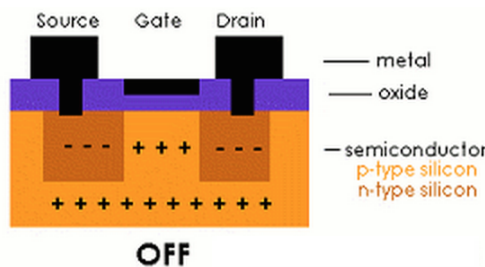
First of all, HEMTs, also called heterostructure FETs (HFETs) or modulation-doped FETs (MODFETs), are field-effect transistors (FETs). A FET has three terminals: source, drain and gate. While a FET is in its functioning state, a current flows between the source and the drain, through a channel. A voltage applied to the gate, which influences the channel conductivity, can control this current. The contact between the semiconductor and the gate should be non-ohmic. As a result, the contact will not have a linear current-voltage (I-V) curve. FETs are known as unipolar transistors due to the fact that the channel conductivity depends only on one type of carrier, which is the majority charge carriers. FETs are characterized by a large input impedance, a good linearity and a negative temperature coefficient, permitting a homogeneous temperature distribution. There are different types of FETs; these are distinguished by the structure of their gate diode. In this research, we will specifically analyze the MISFETs (Metal-Insulator-Semiconductor FET). The MISFETs have a metal-insulator-semiconductor gate diode (Figure 1).



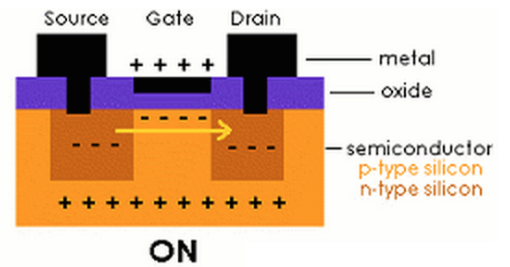
**Figure 1.** Scheme of a MOSFET with channel length  $L$  and oxide thickness  $d$ . The dark grey areas are ohmic metal contacts [8].

If the insulator of a MISFET is an oxide, the device is called a MOSFET (Metal-Oxide-Semiconductor FET). The semiconductor of a MOSFET is constituted of n-type and p-type regions. The regions underneath the source and the drain are heavily doped by conducting electrons, creating n-type regions, and the rest of the semiconductor is heavily doped by electron holes creating p-type regions. Even though there are conducting electrons in the n-type regions, they cannot flow between the source and drain due to the holes present in the p-type gate between the two n-type regions (Figure 2). However, if a positive voltage is applied to the gate (for a p-channel), we observe the formation of an inversion layer close to the insulator-semiconductor interface. This layer creates an n-conductive channel, and enables the electron flow between the two oppositely doped pn-diodes. This process is called the “field-effect” and turns the transistor on (Figure 3), which enables the transmission of a high current.

FETs can be n-type or p-type, depending on the conductivity type of the channel. An n-channel is usually preferred for high-frequency applications, due to the higher mobility or drift velocity. When we have an n-channel conductive at  $V_G = 0V$ , we call it an ‘n-type, normally on’ (or depletion) FET. If the channel is p-conductive, the FET is called ‘p-type’. A FET that has a nonconductive channel at  $V_G = 0$  is called ‘normally off’ (or accumulation) FET.



**Figure 2.** MOSFET in mode Off [7].



**Figure 3.** MOSFET in mode On [7].



Moreover, a HEMT is a FET, for which the channel is generated by the heterojunction of two materials instead of a doped region. The heterojunction is obtained between two materials having a different band gap. Generally, GaAs and AlGaAs material combinations are used in HEMTs, but many different combinations can be found in various application domains of HEMTs. Devices having more indium are usually characterized by a better high-frequency performance. However, during the past few years, GaN HEMTs have attracted attention with their high-power performance. HEMT is a type of transistor used in high-frequency products like cell phones, voltage converters, radar equipment and satellite television receivers, mainly because of the operability of HEMTS at higher frequencies than ordinary transistors.

## **2.2 Advantages of GaN-Based Transistors**

We can find in Table 1 the advantages of GaN devices and amplifiers versus other competitive materials. We notice that in each category, GaN surpasses the conventional technology. In the last column, the performance advantages of GaN devices are highlighted. We can see that the latter offers the most significant product benefits.

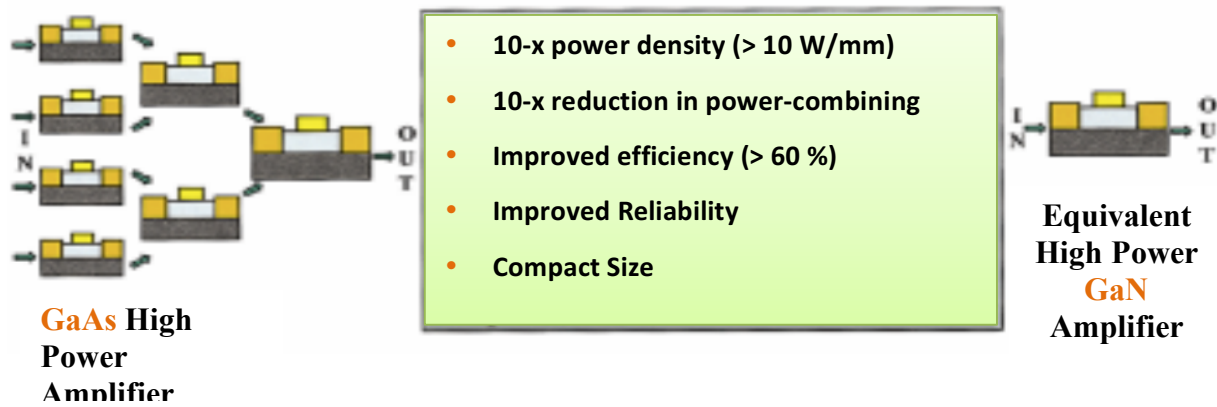
We will take a close look into the performance advantages of GaN devices offered for every need cited in the first column. The high power per unit width enables us to fabricate smaller devices with very high impedances. Thereby, the system match is more easily obtained, which is usually more complex to put in place with conventional devices in gallium arsenide (GaAs).

**Table 1.** Competitive Advantages of GaN Devices [18]

Need	Enabling Feature	Performance Advantage
High Power/Unit Width	Wide Bandgap, High Field	Compact, Ease of Matching
High Voltage Operation	High Breakdown Field	Eliminate/Reduce Step Down
High Linearity	HEMT Topology	Optimum Band Allocation
High Frequency	High Electron Velocity	Bandwidth, $\mu$ -Wave/mm-Wave
High Efficiency	High Operating Voltage	Power Saving, Reduced Cooling
Low Noise	High Gain, High Velocity	High dynamic range receivers
High Temperature Operation	Wide Bandgap	Rugged, Reliable, Reduces Cooling
Thermal Management	SiC Substrate	High Power Devices with Reduced Cooling Needs
Technology Leverage	Direct Bandgap; Enabler for Lighting	Driving Force for Technology; Low Cost

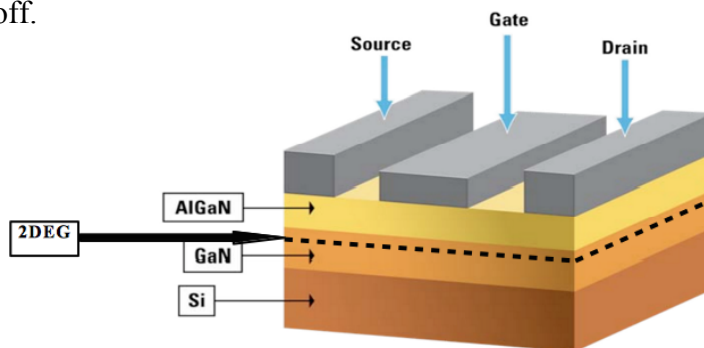
The high voltage characteristic of GaN devices eliminates or reduces the need for voltage conversion. Commercial systems operate at 28 V, and a low-voltage technology would need a voltage conversion from 28 V to the required voltage. Nonetheless, GaN devices can operate at 28 V or more, up to 42 V. As an advantage of this high operating voltage, we get a higher efficiency, which decreases power needs and makes cooling simpler. Since cost and weight of cooling systems constitute a large portion of the price of a high-power microwave transmitter, higher efficiency is an important advantage of GaN devices.

Throughout these past six years, GaN-based HEMTs showed that they have one-order higher power density and efficiency compared to existing technologies [18]. Therefore, GaN-based devices can be ten-times smaller, compared to conventional devices, for the same output power. In figure 4 we see an illustration of how a complex module can be replaced by a smaller module using GaN. The advantages cited in figure 4 are due to the wide bandgap of GaN and the availability of the AlGaIn/GaN heterostructure where high voltage, high current, and low on-resistance can be simultaneously achieved.



**Figure 4.** Schematic comparison illustrating advantages of GaN over existing technology [18].

Furthermore, GaN is naturally piezoelectric, meaning that when a crystal is strained it will produce a small voltage. If we add a very thin layer of AlGaN to the surface of GaN, we can create a lot of strain over very small distance. The latter creates an electric field and better tracks electrons to the interface, creating a 2D electron Gas or 2DEG. The 2DEG is a gas of electrons free to move in two dimensions, but tightly confined in the third. This conductive 2DEG can be used to conduct large amounts of current. It can also be turned off by applying a voltage that tracks away or depletes the electrons. This kind of device is called a depletion mode, or Normally On device. We can see a simple structure of a basic GaN HEMT transistor in figure 5. This structure lets us create a high voltage, high power device. Source, gate and drain terminals are added to conduct electrons, supplied by the 2DEG. The gate terminal can be used to turn the 2DEG on or off.



**Figure 5.** Basic HEMT GaN transistor [11].

In short, GaN devices have great performance and size advantages compared to silicon. These advantages can be applied to gain efficiency advantages, size advantages, or a combination of both, without having a difference in application requirements with silicon [4].

### 2.3 Bottlenecks of GaN HEMT Technology

While GaN HEMT transistors present many advantages, there are several bottlenecks, which will be discussed in this section. There are three main categories that affect lifetime and accelerate the degradation of GaN HEMTs: contact degradation, hot electron effect and inverse piezoelectric effect [3].

Below 300 °C, Schottky<sup>1</sup> and ohmic contacts have great stability. Unfortunately, with an increasing temperature we may observe an increase in contact resistance and passivation cracking caused by gallium (Ga) out-diffusion and gold (Au) inter-diffusion after a 100h thermal storage test stress [15]. If we have Schottky contacts based on nickel, the formation of nickel nitrides on GaN can be seen at temperatures such as 200 °C. The latter causes a decrease in Schottky barrier height [15]. As AlGaIn/GaN HEMT transistors are used in power applications, adequate management of temperature is an important issue which influences the device performance when subjected to high voltage, high current operations. If the cooling mechanisms are not efficient, the self-heating of the device can cause contact degradation and consequently decrease the device performance highly.

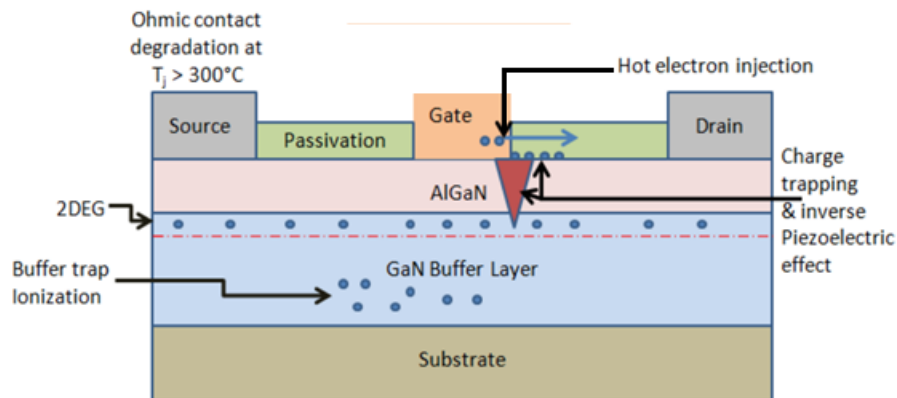
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<sup>1</sup> A **Schottky contact** is a “metal-semiconductor contact having a large barrier height and low doping concentration that is less than the density of states in the conduction band or valence band” [17].

When AlGaIn/GaN HEMT transistors are tested under high voltage, high current operation, we observe a current collapse and gate lag due to hot electrons. Hot electrons are electrons with a very high kinetic energy gained from their acceleration in an important electric field. These electrons are a source of trap formation in the AlGaIn layer and the buffer [15]. As a consequence of this trap generation, a larger depletion region is formed between the gate and drain terminals. This increases the drain resistance and decreases the saturated drain-source current. On the other hand, when the GaN HEMT is under “off-state” conditions, there are fewer electrons in the channel resulting in a very small increase in trap generation, which reduces the degradation.

The piezoelectric nature of the GaN mentioned above has a lot of advantages, but besides all of these, there is also a disadvantage, which we will discuss further on. The electric field created by the strained AlGaIn adds more tensile stress to the AlGaIn layer, which can cause irreversible damage to the device when a “critical voltage” is reached. The elastic energy found in AlGaIn/GaN layers surpasses a critical value when electric stress is applied to the device. Electron leakage may occur because of the damage [15].

A representation of the cited failure mechanisms in AlGaIn/GaN HEMTs under electrical stressing conditions at typical operating temperatures can be found in figure 6.



**Figure 6.** Schematic of degradation mechanisms in AlGaIn/GaN HEMTs [3].

## 2.4 Solutions for Bottlenecks of GaN HEMT Technology

One of the solutions proposed to reduce the inverse piezoelectric effect and to increase the off-state breakdown voltage of AlGaIn/GaN HEMTs is to use a source field plate, which can also be seen as an addition of a novel electrode. The fabrication of a source field plate over the gate electrode decreases the maximum electric field between the drain and the gate. The latter is the reason for the increase in off-state breakdown voltage.

The type of gate metal used in HEMTs plays an important role in device reliability. HEMTs with Ni/Au gate metallization wafer have a much lower critical voltage compared to Pt/Ti/Au gate metallization. We can say that Pt based gate metallization has a better performance in the operating bias conditions and improves device reliability. Bias stressing does not much affect Schottky barrier height and ideality of Pt/Ti/Au compared to Ni/Au gate metallization, which presents higher gate reverse bias leakage current, and much lower breakdown voltage [3]. We can conclude that Pt has better stability, but there is still a problem that persists: peel-off of the contact metal due to stress in the metal.

The substrate choice for AlGaIn/GaN HEMTs is an important concept that affects the off-state degradation of GaN devices. The degradation in GaN devices grown on SiC substrate is believed to be related to the generation of percolation paths due to defects in the AlGaIn barrier or threading dislocations in the device epilayers [9]. A new possible substrate choice competitive with SiC and Si is bulk-GaN substrate. One of the advantages of having a bulk-GaN substrate compared to Si and SiC is the fact that the nucleation layer is not necessary for device growth. Another advantage is that bulk-GaN substrate has a high thermal conductivity. The latter makes GaN-on-GaN devices thermally competitive to GaN-on-SiC one. Moreover, using a bulk-GaN

substrate lets us have several orders of magnitude lower dislocation densities than GaN-on-SiC, and therefore eliminates one of the possible causes of device degradation [9]. GaN-on-GaN devices are ideally suited for device degradation analysis because they are less influenced by threading dislocations. A study of GaN-on-GaN devices showed that the surface microstructure plays an important role on off-state degradation [9]. GaN-on-GaN HEMTs can be used to minimize the impact of step edges causing device failure and to optimize epilayers in order to obtain highly reliable GaN electronic devices.

### 3 Description of Research Results

#### 3.1 Research Goals Overview

This research primarily consists of simulating AlGa<sub>N</sub>/Ga<sub>N</sub> based power transistors in order to understand their different characteristics, such as voltage-current relations, using TCAD Sentaurus software. It will also investigate the change in the breakdown voltage with different design strategies of AlGa<sub>N</sub>/Ga<sub>N</sub> HEMTs. Increasing the breakdown voltage would eliminate the damage due to the latter in high voltage, high current applications and to extend the lifetime and operating bias conditions.

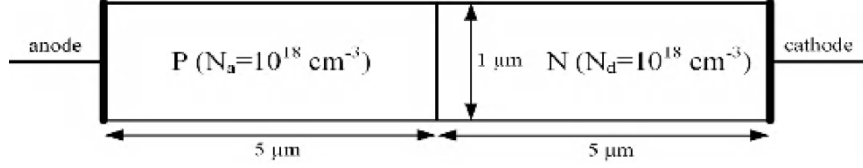
TCAD Sentaurus device simulator developed by Synopsys is a widely used commercial device simulation tool. Sentaurus is based on TAURUS MEDICI, which is derived from a software developed by Stanford University, PISCES, and from device simulator DESSIS by ISE. TCAD Sentaurus has been an essential tool for studying theoretical aspects of Ga<sub>N</sub> based HEMTs, such as breakdown characteristics depending on surface defect charges, hot electron effects, and self-heating and current collapse effects.

The main reason in choosing TCAD Sentaurus software for my simulations is the fact that Sentaurus is widely used in Ga<sub>N</sub> HEMT theoretical studies and is one of the most developed and professional softwares in this domain. Another reason in choosing this software is the opportunity to use this expensive software free on Engineering Work Stations at UIUC.



## 3.2 Work and Contributions

### 3.2.1 Simulation of a P-N Junction



**Figure 7.** Dimensions and doping of the p-n junction diode used during the simulations.

To start with, a basic p-n junction is simulated using the TCAD Sentaurus platform. The main reason being to increase general knowledge on the tool by being able to compare the characteristics obtained during the simulation against the well know theoretical ones.

A silicon p-n junction doped with boron on the p-side and doped with arsenic on the n-side, each with a concentration of  $10^{18} \text{ cm}^{-3}$ , is used throughout the simulations. The diode has a total length of  $10 \mu\text{m}$ , a height of  $1 \mu\text{m}$  and a depth of  $1 \mu\text{m}$  (cf. Figure 7). A 2D simulation is enough for analyzing the characteristics of the diode.

The first simulation setup that is studied is the meshing strategy.. The correct choice of meshing reduces possible errors during simulations. The strategy used on the p-n junction is to define two different meshing types: a fine mesh near the junction and a coarse mesh for the rest of the device. Only the mesh size in the x-direction is adjusted, as the device is uniform in the y-direction. Near the depletion region, the mesh spacing in the x-direction has to be smaller than the depletion width in order to reduce simulation errors. Depletion width is calculated using equation (3.1).

$$W = \sqrt{\frac{2\epsilon \cdot kT \cdot \ln\left(\frac{N_a \cdot N_d}{n_i^2}\right) \left(\frac{1}{N_a} + \frac{1}{N_d}\right)}{q^2}} \quad (3.1)$$

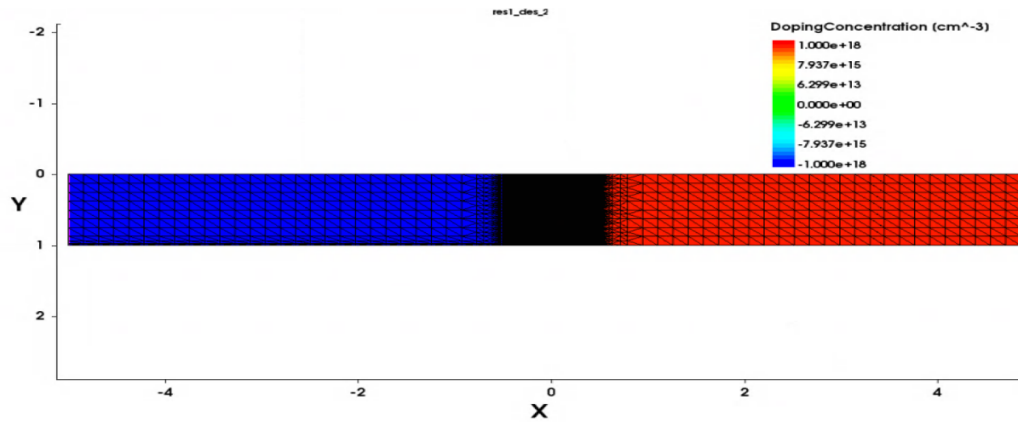
In equation (3.1),  $\epsilon$  is the multiplication of the permittivity of free space  $\epsilon_0$  and the material used in junction fabrication  $\epsilon_r$ . As the simulations are made using a silicon-based p-n junction we have  $\epsilon_r = 11.8$  and  $\epsilon_0 = 8.85418782 \times 10^{-12}$  F/m. Temperature  $T$  is assumed to be equal to room temperature (300 K). The Boltzmann constant  $k$  is equal to  $1.3806488 \times 10^{-23}$  J/K. The intrinsic carrier concentration  $n_i$  of silicon at room temperature is  $1.45 \times 10^{10}$  cm<sup>-3</sup>. Charge of an electron  $q$  is defined as  $1.60217662 \times 10^{-19}$  C.

By doing a numerical application, the depletion width  $W$  of the p-n junction is found to be  $0.049 \mu\text{m}$ . Therefore, a mesh size of  $0.01 \mu\text{m}$  in the x-direction is enough for our simulations. We can see in figure 8 that the meshing near the junction is much denser than the meshing present on the rest of the device. The coordinate system is set to have the junction located at  $x=0$ .

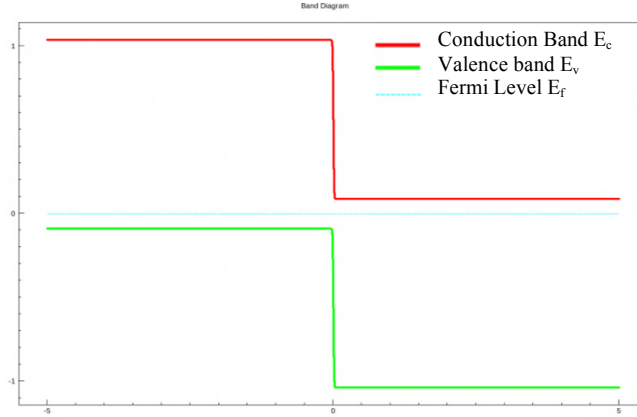
Next, the band-diagrams, built-in electric fields and built-in potentials of the junction in equilibrium, forward bias and reverse bias conditions are studied.

When the junction is in equilibrium, no potential is applied to its terminals. The Fermi level is constant. The band diagram of the junction at equilibrium can be seen in figure 9.

The Fermi level for electrons  $E_{Fn}$  is the same as the Fermi level for the holes  $E_{Fp}$  for the junction in thermal equilibrium, which is in accordance with our theoretical knowledge.



**Figure 8.** P-N junction simulated with TCAD showing the meshing and doping concentrations.



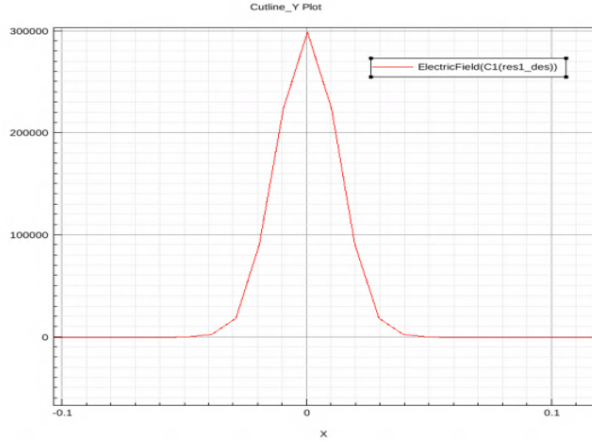
**Figure 9.** Band diagram of the p-n junction at equilibrium

The valence band  $E_v$  is closer to the Fermi level for negative values of  $x$ , which shows that the junction is p-type doped in that region. In contrast, the conduction band  $E_c$  is closer to the Fermi level for positive  $x$  values, which shows that the junction is n-type doped in that region. As the Fermi level should remain constant throughout the junction, there is a distortion of valence and conduction bands.

Next, the built-in electric field in the depletion region is analyzed. The electric field within the depletion region is characterized by equation (3.2). Outside the depletion region as we have neutral p and n regions, the electric field is zero.

$$E(x) = \begin{cases} \frac{q \cdot N_d}{\epsilon} (x - x_{n0}) & 0 < x < x_{n0} \\ -\frac{q \cdot N_a}{\epsilon} (x + x_{p0}) & -x_{p0} < x < 0 \end{cases} \quad (3.2)$$

TCAD Sentaurus takes the absolute value of the electric field for its plots. That is the reason why we have positive electric field displayed on our plots, as can be seen in figure 10. We can observe that the electric field is more or less symmetrical with respect to y-axis. The latter is due to the fact that the n and p sides are equally doped.



**Figure 10.** Electric field within the depletion region for the simulated p-n junction in equilibrium

We observe from our simulations that the maximal electric field  $E_0$  is more or less equal to  $3 \times 10^5$  V/cm. We should compare this value with the theoretical  $E_0$  calculated using equations (3.3) and (3.4). By doing a numerical analysis, we get for maximum electric field:

$$|E_0|_{\text{theory}} = 3.753 \times 10^5 \text{ V/cm}$$

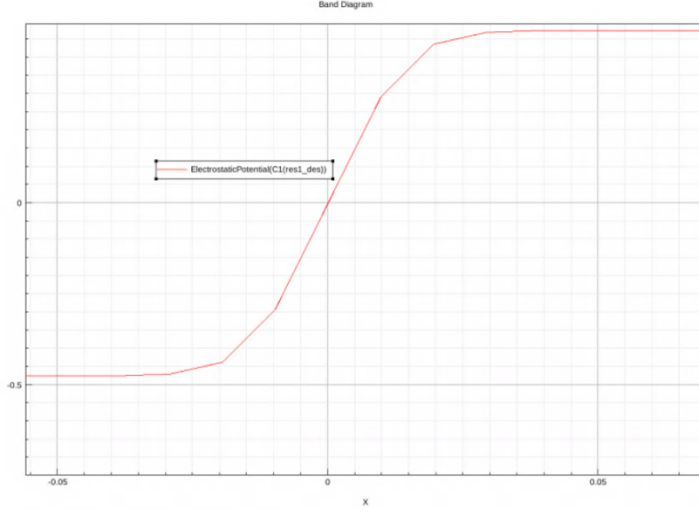
With TCAD, we have an error of 20% for  $E_0$ , which we cannot consider as a good approximation.

$$|E_0| = \left| \frac{q * N_d}{\epsilon} (-x_{n0}) \right| = \left| -\frac{q * N_a}{\epsilon} (x_{p0}) \right| \quad (3.3)$$

$$x_{n0} = \frac{W}{1 + N_d/N_a} \text{ and } x_{p0} = \frac{W}{1 + N_a/N_d} \quad (3.4)$$

The built-in potential in the depletion region can be found using equation (3.5). TCAD gave us the plot for the built-in potential seen in figure 11.

$$V(x) = \begin{cases} -\frac{q * N_d}{\epsilon} \left( \frac{x^2}{2} - x_{n0} * x \right) & 0 < x < x_{n0} \\ \frac{q * N_a}{\epsilon} \left( \frac{x^2}{2} + x_{p0} * x \right) & -x_{p0} < x < 0 \end{cases} \quad (3.5)$$



**Figure 11.** Built-in potential of the p-n junction within the depletion region in equilibrium

The total potential over the junction  $V_0$  is the difference between  $V(-x_{p0})$  and  $V(x_{n0})$ . From the plot we obtained using TCAD we can deduce that:

$$V_0 = 0.9 \text{ V}$$

Theoretically, we have:

$$V_0 = \frac{qN_d x_{n0}^2}{2\epsilon} + \frac{qN_a x_{p0}^2}{2\epsilon} = 0.919 \text{ V} \quad (3.6)$$

Theoretical  $V_0$  that we calculated is similar to the  $V_0$  we obtained from TCAD plot.

After the equilibrium analysis of the p-n junction, a closer look is given to the change in characteristic of the junction in reverse-bias conditions..

When a junction is reverse-biased, it is subjected to a negative voltage across its terminals. The depletion width gets larger as the reverse-bias voltage gets higher. The increase in depletion width causes an increase in built-in electric field and in built-in potential.

The Fermi level is no longer constant. We have to consider the quasi-Fermi levels in p-side and n-side of the junction.

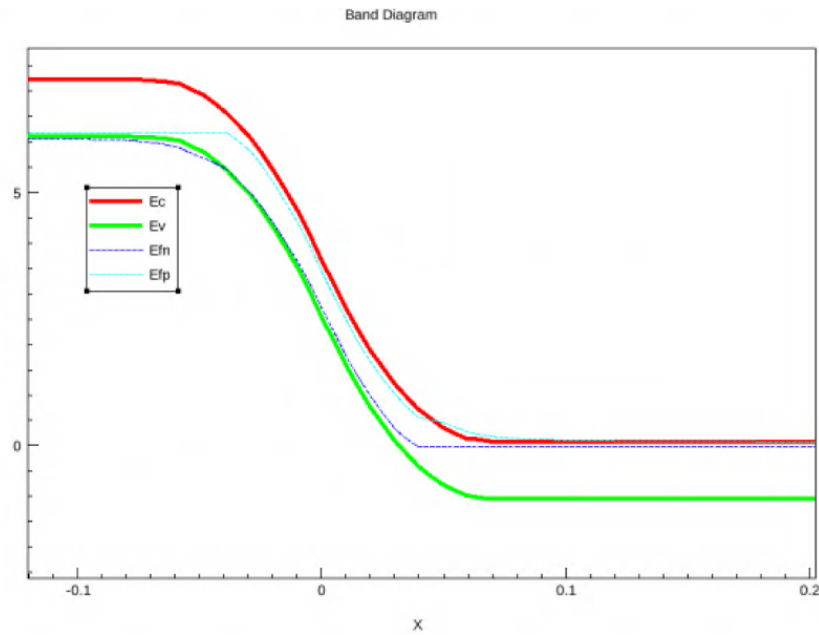
The simulation using TCAD gave the plot of band diagram seen in figure 12. The continuation method is used to simulate the reverse-bias voltage of -10 V applied at the terminals of the junction. Plot obtained in figure 12 is in accordance with the theory.

The built-in electric field and built-in potential graphics acquired from our simulations with a reverse-bias voltage applied at the terminals of the junction can be found in figures 13 and 14. The first observation we can make is that the maximum electric field and the total potential over the junction have increased compared to the equilibrium state. Now we have:

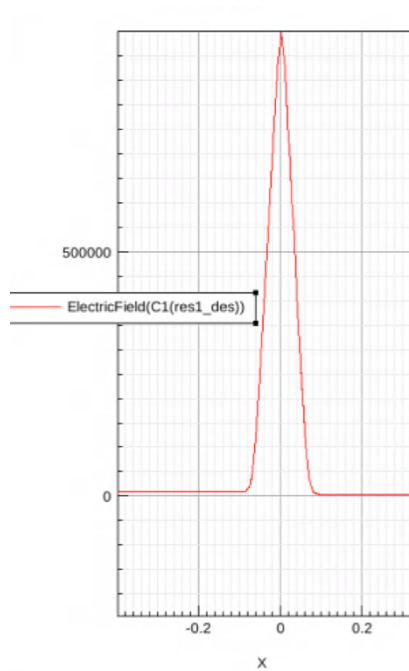
$$|E_0| = 9 \times 10^5 \text{ V/cm}$$

$$V_0 = 7.1 \text{ V}$$

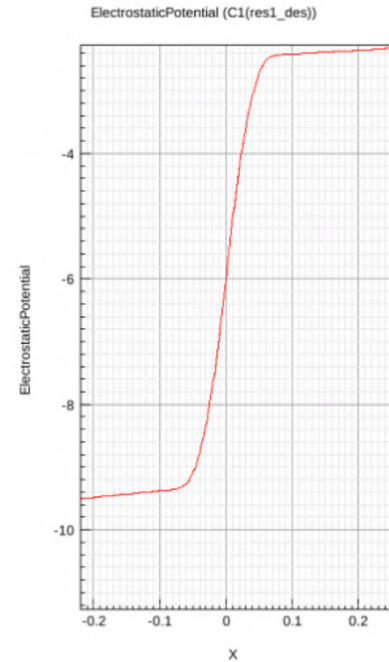
This increase is expected theoretically.



**Figure 12.** Variation of quasi-Fermi levels in a reverse-biased p-n junction simulated with TCAD.

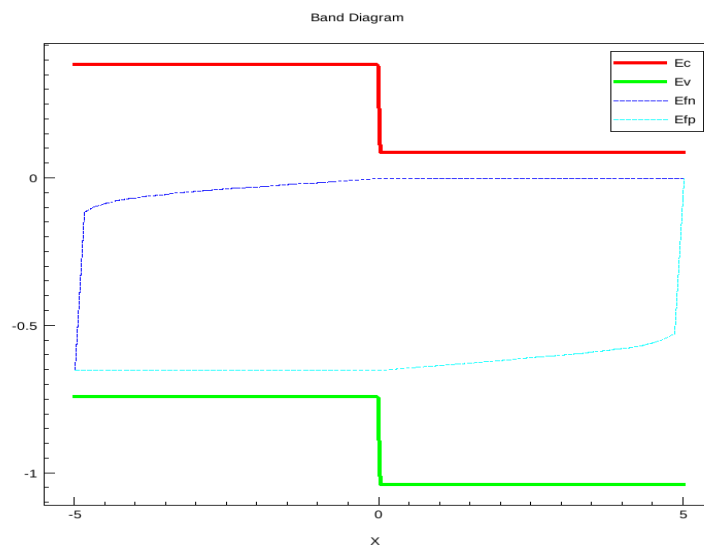


**Figure 13.** Built-in electric field of the p-n Junction in reverse-bias.



**Figure 14.** Built-in potential of the p-n junction in reverse-bias.

Finally, the p-n junction junction is simulated in forward bias. The method used in TCAD is the “QuasiStationary” function, which is used to increase the potential on the anode from 0 to 0.65 V. By doing so we expect to have a decrease in the width of the depletion region, causing a decrease in electric field and in built-in potential. The simulated band diagram of the forward biased junction can be found in figure 15. Plot obtained in figure 15 is in accordance with the theory.

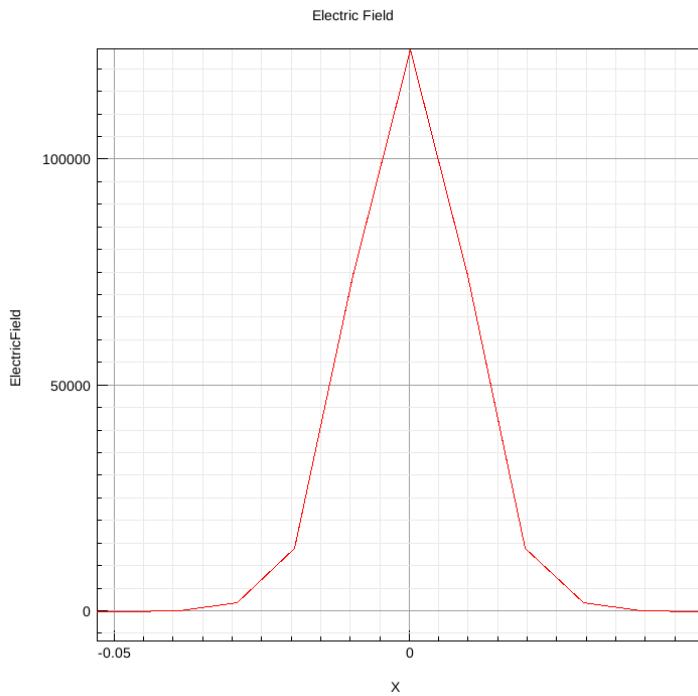


**Figure 15.** Band diagram of p-n junction simulated in forward bias conditions.

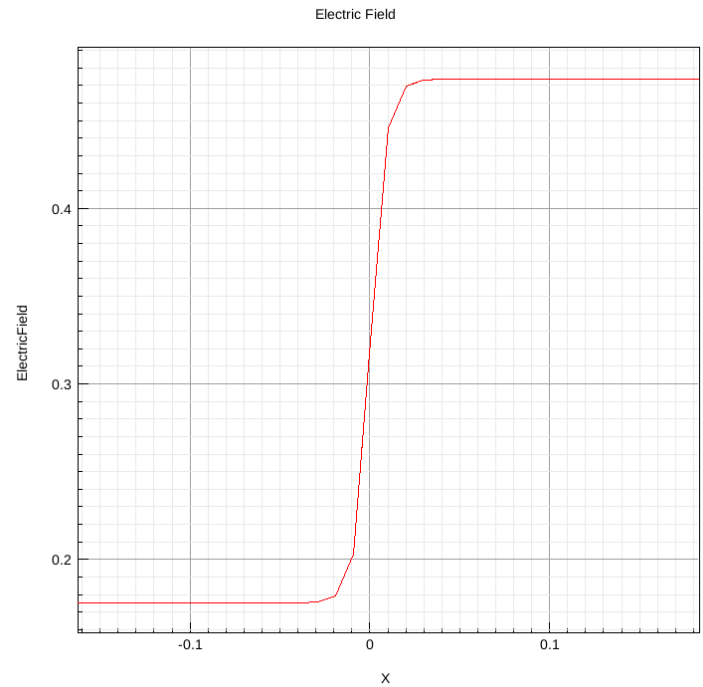
The built-in electric field and built-in potential graphics acquired from our simulations with a reverse-bias voltage applied at the terminals of the junction can be found in figures 16 and 17. As expected, the maximum electric field and the total potential over the junction has decreased compared to the equilibrium state. Now we have:

$$|E_0| = 1.25 \times 10^5 \text{ V/cm}$$

$$V_0 = 0.3 \text{ V}$$



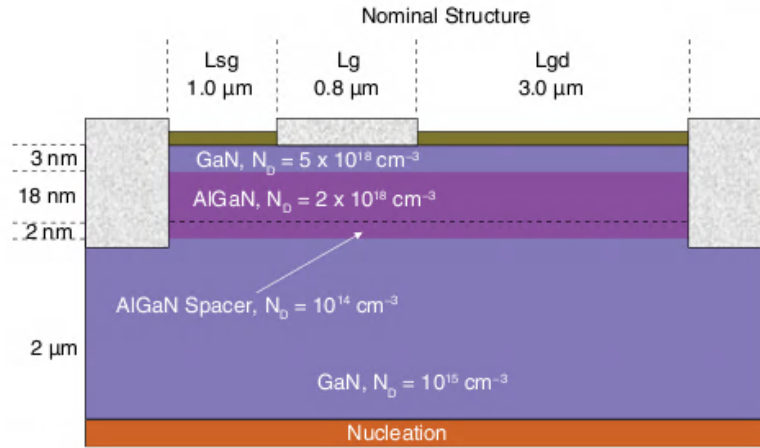
**Figure 16.** Built-in electric field of the p-n Junction in forward bias.



**Figure 17.** Built-in potential of the p-n junction in forward bias.



### 3.2.2 Simulation of GaN-Based Heterojunction FET (HFET)

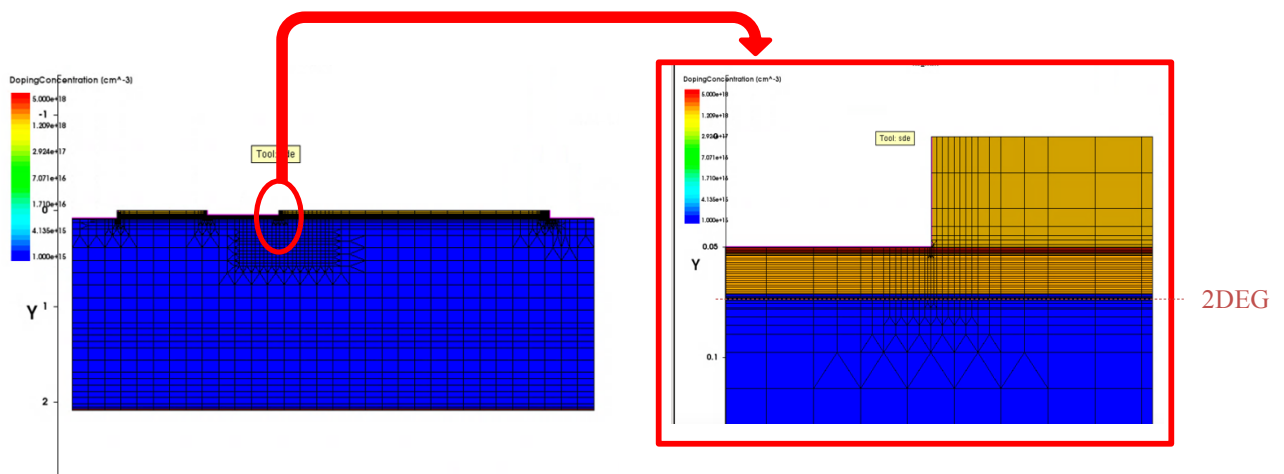


**Figure 18.** Model Structure used in simulations: doping and dimensions are indicated.

In this section the simulation of the GaN HFET provided by TCAD Sentaurus software is covered. The structure of the GaN HFET can be seen in Figure 18 [14].

The simulation of ohmic contacts is made by applying a high doping around the source and drain terminals, although the latter is not physically correct.

It can be seen in Figure 19 that the meshing is denser at heterointerfaces, where the carrier concentration has a large variation within a short distance, like in the 2DEG.

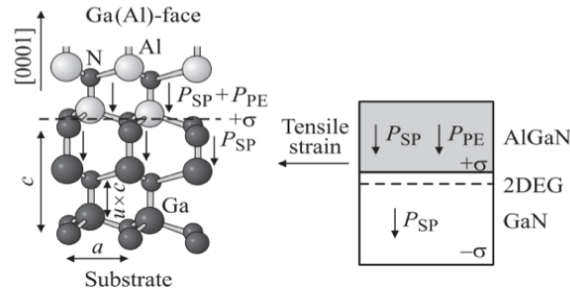


**Figure 19.** Visualization of the meshing.

Epitaxial growth of polarized Wurtzite crystal structures is assumed to be [0001] Ga-face oriented (cf. figure 20). The 3D Cartesian coordinates used to define the polarization model should be rotated in order to have a correct model for 2D simulations. The c-axis must be parallel to y-axis. Thence, all the materials and regions in the structure have the same orientation. TCAD Sentaurus uses a built-in polarization model that takes into consideration the spontaneous and piezoelectric components [10], as well as the converse piezoelectric effect that reduces the polarization [1]. The piezoelectric (strain-induced) polarization model used by TCAD Sentaurus calculates the c-axis component of the polarization vector, denoted as  $P_Z$ . The expression used for  $P_Z$  can be found in equation (3.7).

$$P_Z = 2 \frac{a_0 - a}{a} (1 - \text{relax}) \left( e_{31} - e_{33} \frac{c_{13}}{c_{33}} \right) + P_{Z_{sp}} \quad (3.7)$$

The computation takes into consideration the material and mole-fraction at every mesh point. “Relax” is a user-defined lattice relaxation parameter. It is set to 0.1 by default.  $P_{Z_{sp}}$  is the spontaneous polarization component,  $a_0$  and  $a$  are the lattice constants of strained and relaxed materials, respectively,  $e_{ij}$  are piezoelectric coefficients, and  $c_{ij}$  are stiffness constants. All the model parameters depending on mole fraction and linear-interpolation are applied between values for GaN ( $x=0$ ) and AlN ( $x=1$ ) [14]. The default values of the parameters can be seen in Table 2.



**Figure 20.** Crystal structure and polarization vectors (spontaneous and piezoelectric components) [16].

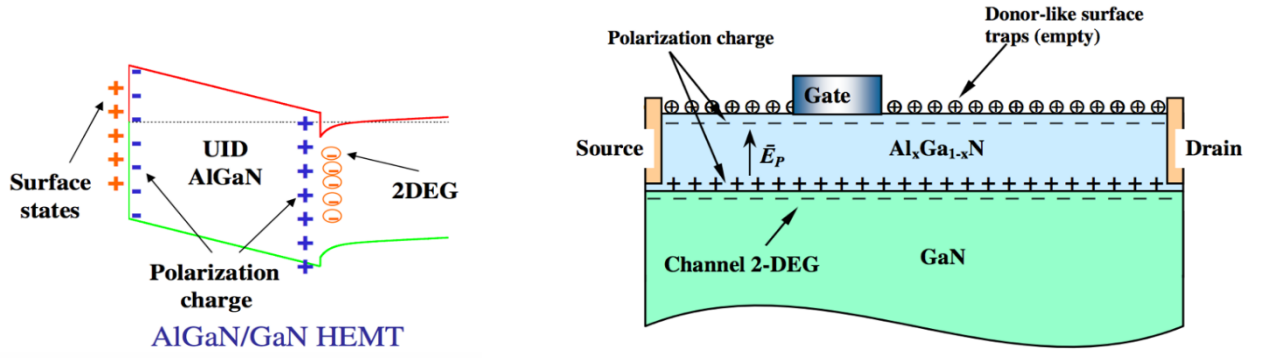
**Table 2.** Parameters for polarization model used in the template [14]

Symbol	Unit	GaN	AlN	InN
$P_{Z_{sp}}$	C/cm <sup>2</sup>	$-2.9 \times 10^{-6}$	$-8.1 \times 10^{-6}$	$-3.2 \times 10^{-6}$
$e_{31}$	C/cm <sup>2</sup>	$-3.50 \times 10^{-5}$	$-5.00 \times 10^{-5}$	$-5.70 \times 10^{-5}$
$e_{33}$	C/cm <sup>2</sup>	$1.27 \times 10^{-4}$	$1.79 \times 10^{-4}$	$9.70 \times 10^{-5}$
$c_{13}$	GPa	106	108	92
$c_{33}$	GPa	398	373	224
$a_0$	Å	3.189	3.189	3.189
$a$	Å	3.189	3.112	3.540
relax	–	0.1	0.1	0.1

The converse piezoelectricity causes an increase in polarization by a factor  $e_{33}^2/c_{33}$ . The latter is taken into account by modifying the z-component (parallel to c-axis) of the anisotropic dielectric tensor within the simulations held by TCAD Sentaurus. The anisotropic Poisson equation used by TCAD Sentaurus is as in equation (3.8) below.

$$\nabla \cdot \begin{bmatrix} \kappa_a & & \\ & \kappa_a & \\ & & \kappa_c + \frac{e_{33}^2}{c_{33}} \end{bmatrix} \nabla \varphi = -\rho + \nabla \cdot \begin{bmatrix} 0 \\ 0 \\ P_z \end{bmatrix} \quad (3.8)$$

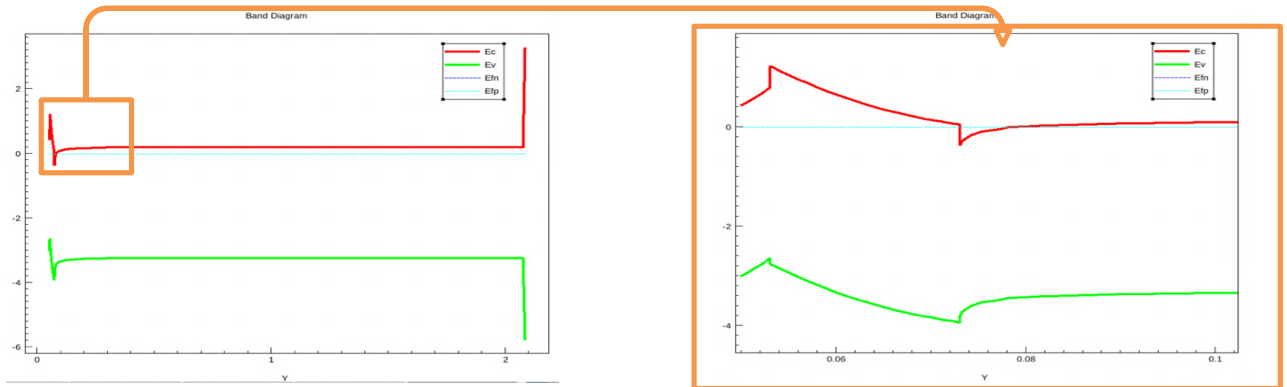
A large polarization divergence is present both at GaN cap-nitride interface and at AlGaN/GaN interface. However, the one at GaN cap surface would cause the production of a large sheet of negative polarization charge. The latter would cause the depletion of electrons present in the channel. In order to prevent the latter from happening, the negative charges at the GaN cap surface should be compensated by other surface charges. In our simulations, we assume that the polarization charge at the surface is completely compensated by interface trap states. To be precise, the compensation is due to deep, single-level trap states, with  $N_{Tsurf} = 5 \times 10^{13} \text{ cm}^{-2}$  and  $E_{Tsurf} - E_i = 0.4 \text{ eV}$ . This phenomenon can be observed in Figure 21.



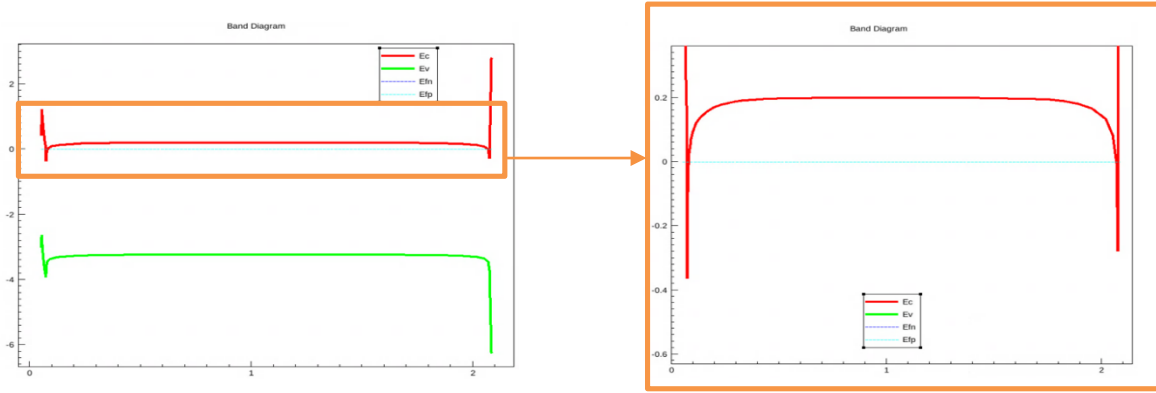
**Figure 21.** Representation of the polarization charges and the 2DEG [6].

We might think that polarization charge present at heterointerfaces below the GaN buffer layer would cause a similar effect of depleting the channel as described above. Nevertheless, polarization charges at these interfaces are usually compensated by charged defects and do not intervene in the electrical operation of GaN HFET devices. Sentaurus Device still gives us the possibility to take into account the polarization charge at GaN buffer-nucleation layer interface, although the latter is set to be zero by default.

The band diagrams of the simulated GaN HFET device when polarization charge at GaN buffer-nucleation layer interface was not-activated and activated can be seen in figures 22 and 23 respectively. The band diagrams are obtained among a vertical cutline drawn from the gate terminal to the nucleation layer, when zero voltage is applied at the gate terminal.



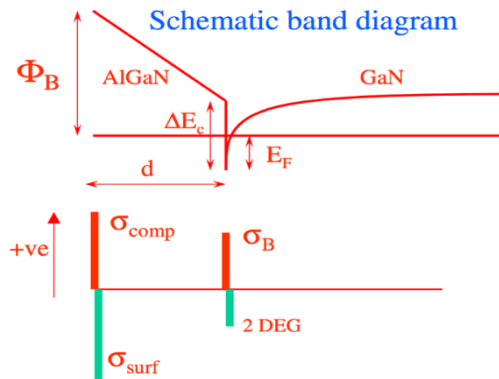
**Figure 22.** Band diagram of the GaN HFET when polarization charge at GaN buffer-nucleation layer interface is ignored.



**Figure 23.** Band diagram of the GaN HFET when polarization charge at GaN buffer-nucleation layer interface is activated.

The first observation we can make is that the band diagram obtained in figure 21 matches with the expected theoretical band diagram, which can be seen in figure 24. The fact that the conduction band energy drops below the Fermi level at the AlGaIn/GaN heterointerface shows us the presence of the 2DEG in absence of an external voltage. Therefore, we have a “normally on” device.

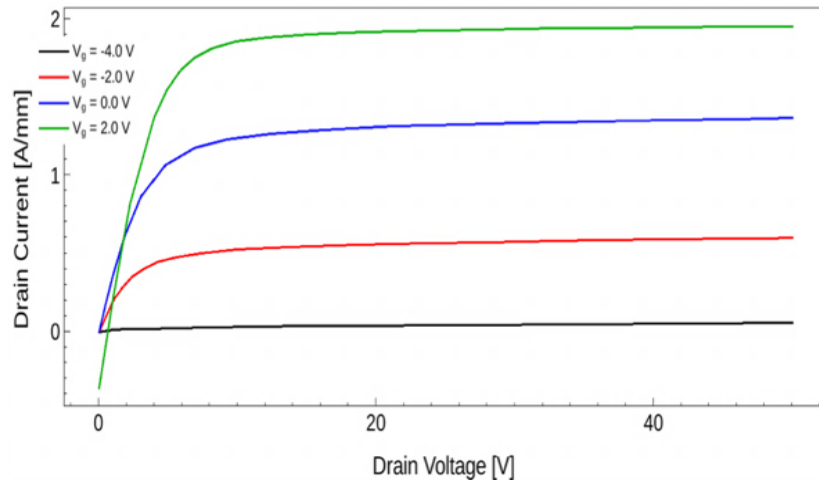
In figure 23, when the polarization charge at the GaN buffer-nucleation layer interface is taken into account, we observe another 2DEG region at the GaN-nucleation interface. The latter has a smaller height than the 2DEG formed at AlGaIn/GaN heterointerface (the  $E_C$  drops below the  $E_F$  deeper at the AlGaIn/GaN interface). This result is expected. It is better to neglect the polarization charge at GaN buffer-nucleation interface.



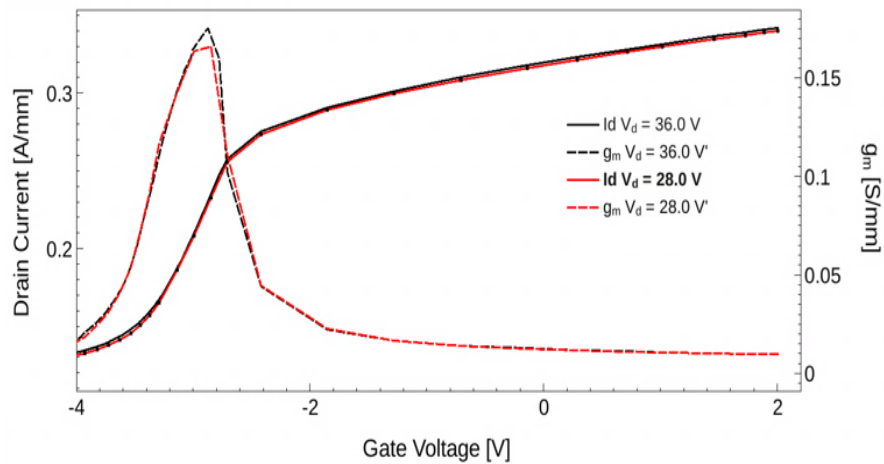
**Figure 24.** Schematic band diagram of the simulated GaN HFET at the AlGaIn/GaN heterointerface [6].

The simulations also provide us  $I_{DS}/V_{DS}$  and  $I_{DS}/V_{GS}$  characteristics of the GaN HFET after a DC analysis of the latter. The gate terminal is ramped from -2 V to +4 V in order to obtain the  $I_{DS}/V_{DS}$  characteristics.  $I_{DS}/V_{GS}$  characteristics are extracted for  $V_{DS}=28$  V and 36 V while  $V_{GS}$  is increased up to 2 V. The results can be found in figures 25 and 26.

The  $I_{DS}/V_{DS}$  characteristics represented in figure 25 confirms that we have a “normally on” device as  $I_{DS}$  is not zero when  $V_{GS}=0$  V.

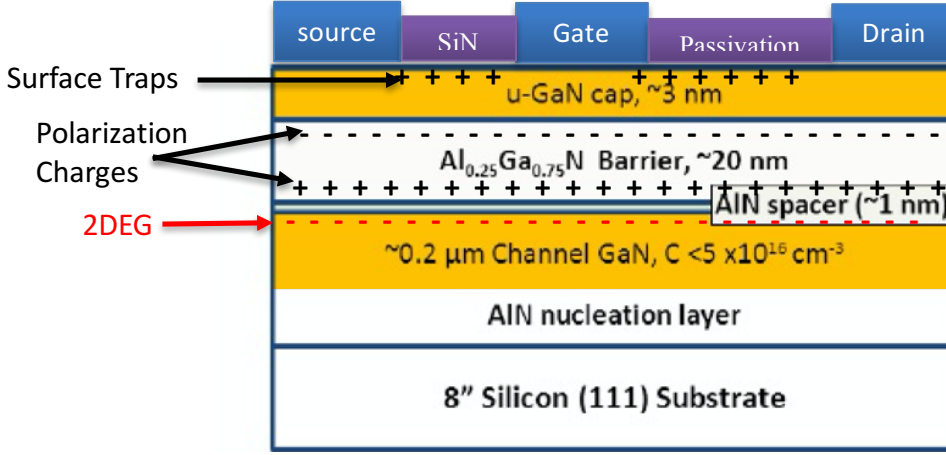


**Figure 25.**  $I_{DS}/V_{DS}$  characteristics of the simulated GaN HFET.



**Figure 26.**  $I_{DS}/V_{GS}$  characteristics of the simulated GaN HFET.

### 3.2.3 Simulation of a GaN Power Transistor



**Figure 27.** Model structure used in simulations: doping and dimensions are indicated.

In this section, the simulation of the breakdown voltage of a GaN-based power transistor, designed by the research group of Prof. Can Bayram, is presented. The structure of this GaN power transistor can be found in figure 27. For simplicity, only the cap, barrier, spacer and channel have been used during the simulations. The current-voltage characteristics of a HEMT depend mainly on the 2DEG, which is formed in the channel. The buffer, nucleation layer and the substrate are not essential for simulations. The values of different parameters used for device simulation can be found in Table 3. The GaN cap is undoped, as well as the AlGaIn barrier. This will reduce the impurity scattering that affects the mobility of the electrons confined in 2DEG.

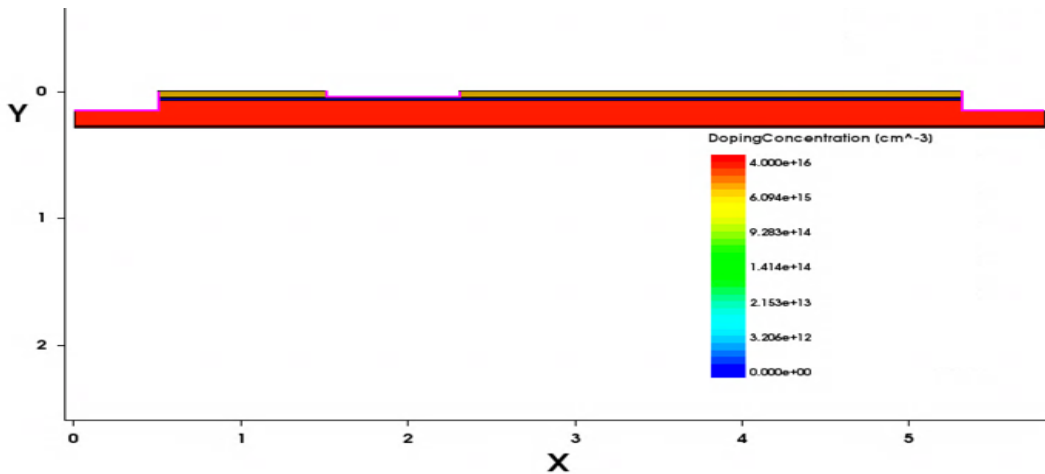
The theory and models used by TCAD Sentaurus in order to simulate the polarization and the formation of the 2DEG resulting from the natural piezoelectricity of III-nitride materials have been discussed in pages 22-24 of this thesis. The polarization charges, surface traps and the 2DEG are represented in figure 27.

**Table 3.** The Structural parameters of HEMT

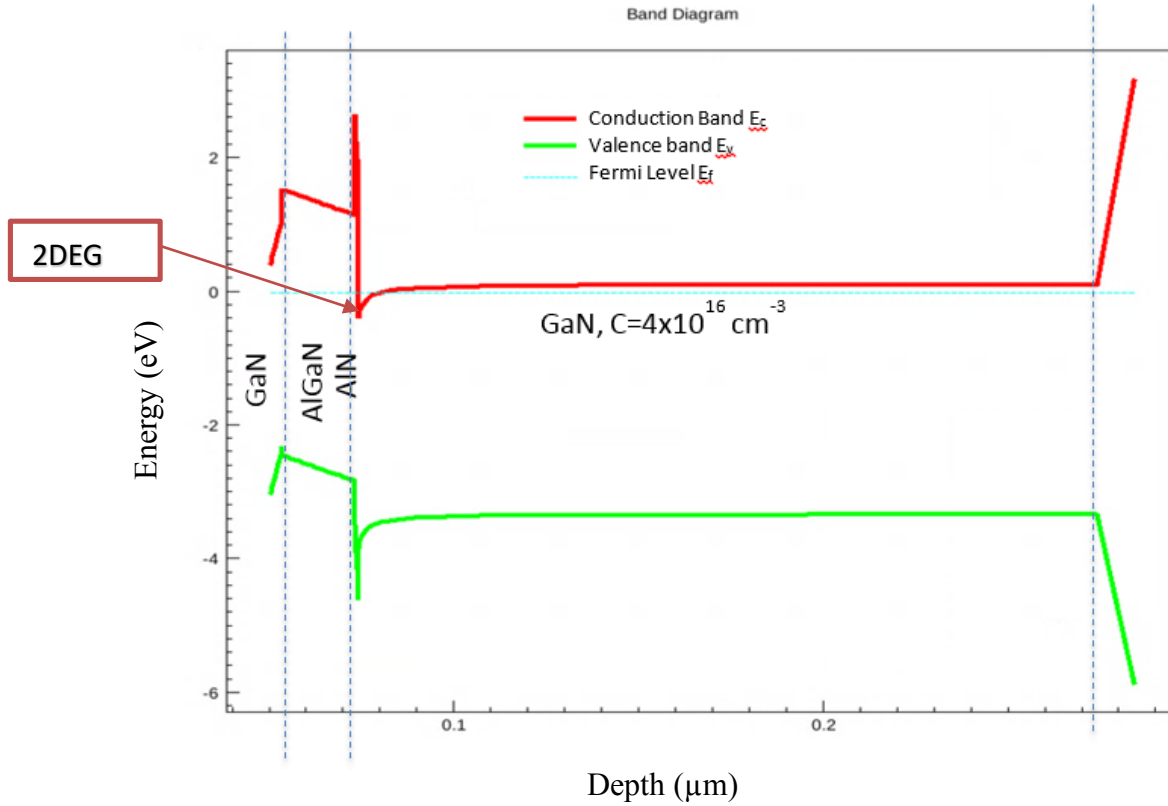
PARAMETER	VALUE
Top Passivation height	50 nm
u-GaN cap layer height	3 nm
AlGaN barrier height	20 nm
AlN spacer height	1 nm
GaN channel height	0.2 $\mu\text{m}$
Gate length ( $L_g$ )	0.8 $\mu\text{m}$
Source length ( $L_s$ )	0.5 $\mu\text{m}$
Drain length ( $L_d$ )	0.5 $\mu\text{m}$
Source-Gate length ( $L_{sg}$ )	1 $\mu\text{m}$
Gate-Drain length ( $L_{gd}$ )	3 $\mu\text{m}$
$x$ mole fraction ( $\text{Al}_x\text{Ga}_{1-x}\text{N}$ )	0.25
Channel doping concentration	$4 \times 10^{16} \text{ cm}^{-3}$

### 3.2.3.1 Device visualization

The simulation of the GaN HEMT model presented in figure 27 gave us the structure in TCAD seen in figure 28. The band diagram, presented in figure 29, is obtained at zero bias conditions. The 2DEG is present on the band diagram more or less at the top of the channel layer as represented in figure 27.

**Figure 28.** Simulated Model structure: doping is indicated.

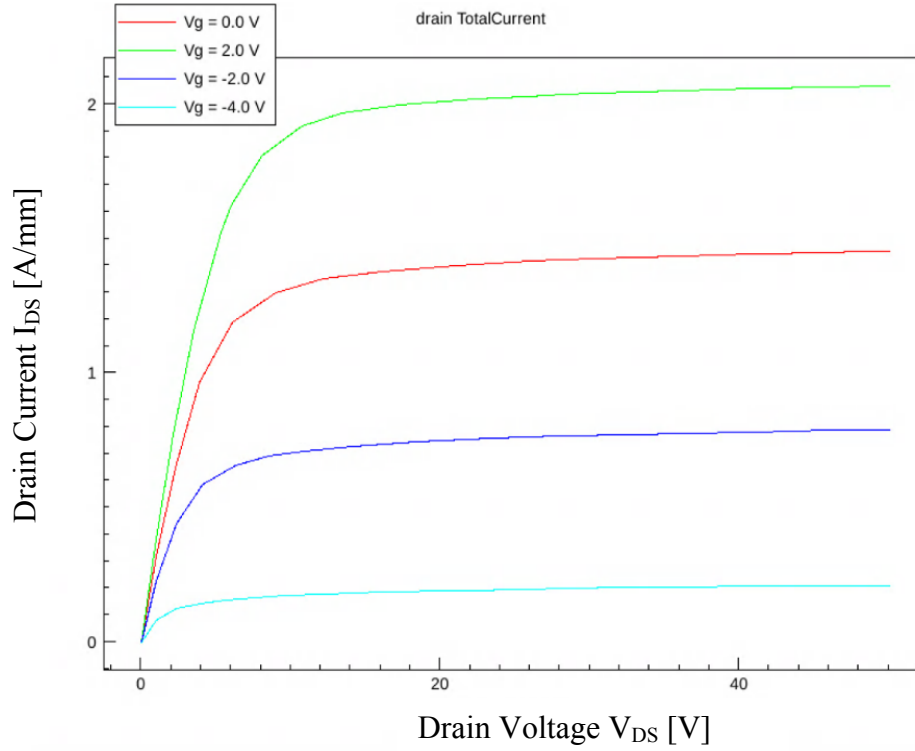




**Figure 29.** Band diagram of GaN HEMT at equilibrium.

### 3.2.3.2 $I_{DS}/V_{DS}$ Characteristics

The simulations provide us  $I_{DS}/V_{DS}$  characteristics of the GaN HFET after a DC analysis of the latter. The gate terminal is ramped from -2 V to +4 V in order to obtain the  $I_{DS}/V_{DS}$  characteristics.  $I_{DS}/V_{DS}$  characteristics for different gate voltages can be found in figure 30. We can observe that as the gate voltage increases, the asymptotic value of the drain current increases as well. As the drain current is not zero at zero bias conditions, we can say that we have a normally on device.



**Figure 30.**  $I_{DS}/V_{DS}$  characteristics of the simulated GaN HEMT

### 3.2.3.3 Breakdown Voltage

The off-state breakdown voltage of the simulated GaN HEMT is found using TCAD. The gate voltage is kept at -6 V in order to have a very small drain current and simulate the off-state of the HEMT.

The cause of the breakdown is defined as avalanche generation (impact ionization). The breakdown is due to charge multiplication which occurs when the width of a space charge region is greater than the mean free path between two ionizing impacts. The reciprocal of the mean free path is called the ionization coefficient  $\alpha$  [13]. The ionization coefficients are defined for electrons and for holes. The generation rate is expressed using these ionization coefficients in equation (3.9).

$$G^{ii} = \alpha_n n v_n + \alpha_p p v_p \quad (3.9)$$

The breakdown simulations with TCAD use the van Overstraeten–de Man model to define threshold behavior of the ionization coefficient (see equations (3.10) and (3.11)).

$$\alpha(F_{ava}) = \gamma a \exp\left(-\frac{\gamma b}{F_{ava}}\right) \quad (3.10)$$

$$\gamma = \frac{\tanh\left(\frac{\hbar\omega_{op}}{2kT_0}\right)}{\tanh\left(\frac{\hbar\omega_{op}}{2kT}\right)} \quad (3.11)$$

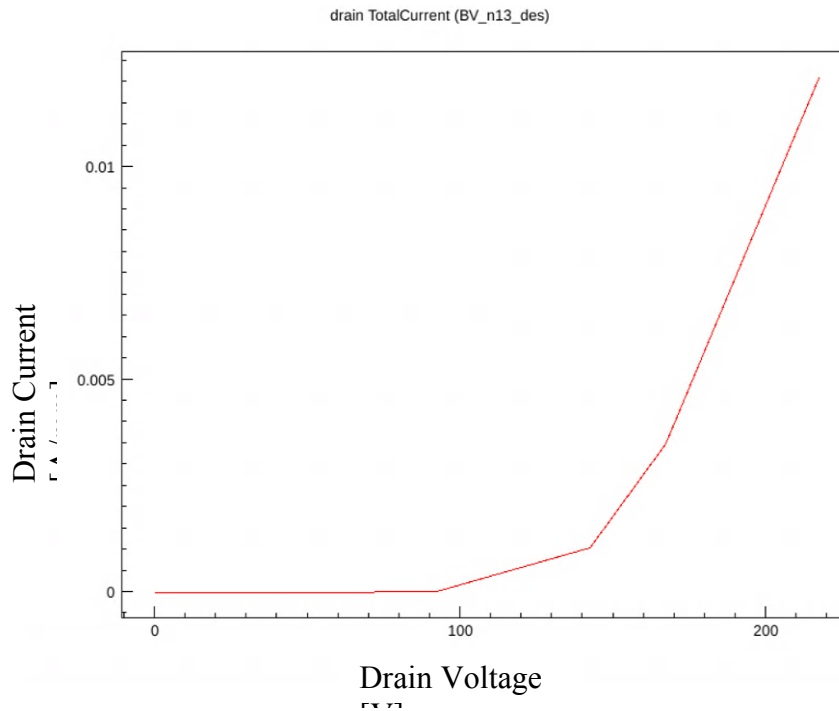
The carriers are accelerated against the phonon gas. The latter has a dependence on temperature, which is expressed by the factor  $\gamma$  and the optical phonon energy  $\hbar\omega_{op}$ . The coefficients  $a$ ,  $b$  and  $\hbar\omega_{op}$  can be found in Table 4. The given values can be used over a field ranging from  $1.75 \times 10^5$  V/cm to  $6 \times 10^5$  V/cm.  $a$  and  $b$  coefficients are defined for high and low ranges of electric field. Low range is from  $1.75 \times 10^5$  Vcm<sup>-1</sup> to  $E_0$ , high range is from  $E_0$  to  $6 \times 10^5$  V/cm [13].

**Table 4.** Coefficients for van Overstraeten–de Man model [13]

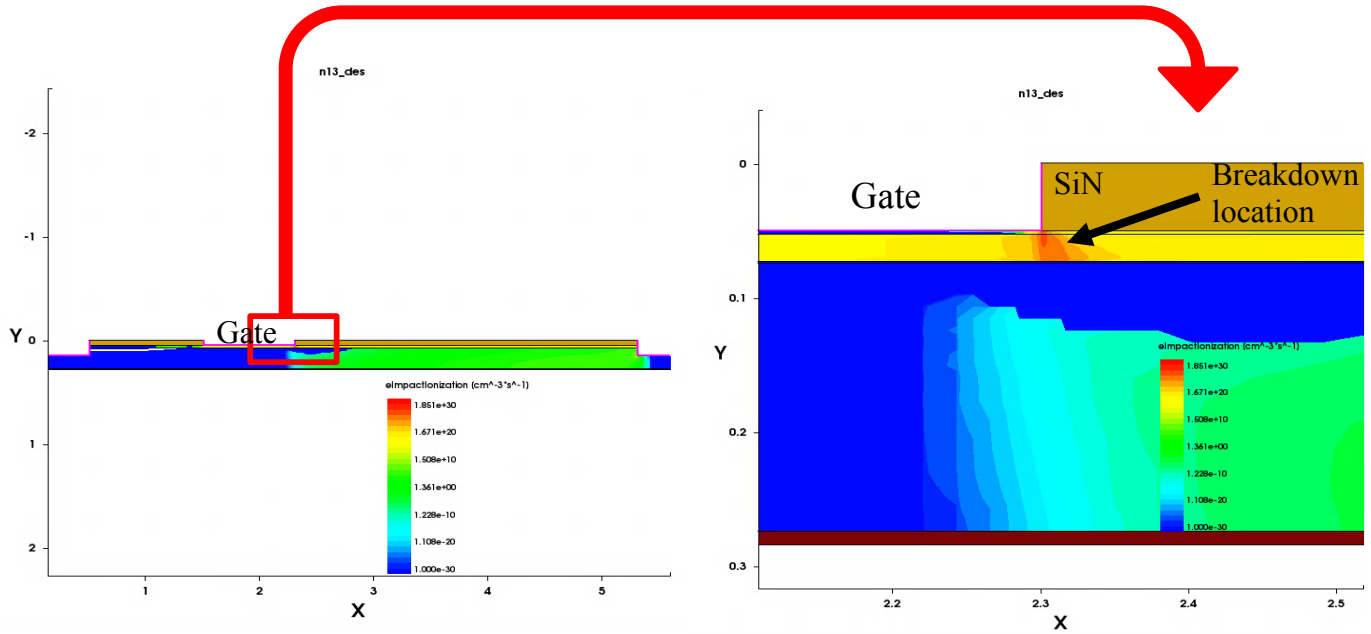
Symbol	Parameter name	Electrons	Holes	Valid range of electric field	Unit
$a$	a (low)	$7.03 \times 10^5$	$1.582 \times 10^6$	$1.75 \times 10^5$ Vcm <sup>-1</sup> to $E_0$	cm <sup>-1</sup>
	a (high)	$7.03 \times 10^5$	$6.71 \times 10^5$	$E_0$ to $6 \times 10^5$ Vcm <sup>-1</sup>	
$b$	b (low)	$1.231 \times 10^6$	$2.036 \times 10^6$	$1.75 \times 10^5$ Vcm <sup>-1</sup> to $E_0$	V/cm
	b (high)	$1.231 \times 10^6$	$1.693 \times 10^6$	$E_0$ to $6 \times 10^5$ Vcm <sup>-1</sup>	
$E_0$	E0	$4 \times 10^5$	$4 \times 10^5$		V/cm
$\hbar\omega_{op}$	hbarOmega	0.063	0.063		eV

The backward Euler method is used to control transient analysis. The break criterion is defined as  $10^{-2}$  A of drain current. The drain voltage is increased until the break criteria is reached. The result of the simulation can be found in Figure 31. We can see that for small values of drain voltage the increase in drain current is invisible; the current seems to be constant. However, after more or less 100 V, even small variations of drain voltage induce a large increase in drain current. This is due to the breakdown of the device. Therefore, we can conclude that the breakdown voltage of the simulated model is close to 100 V.

The visualization of impact ionization when the device breaks down can be found in figure 32, in which it can be seen that the breakdown location is situated at the corner of the gate terminal.



**Figure 31.** Off-state breakdown voltage simulation results.



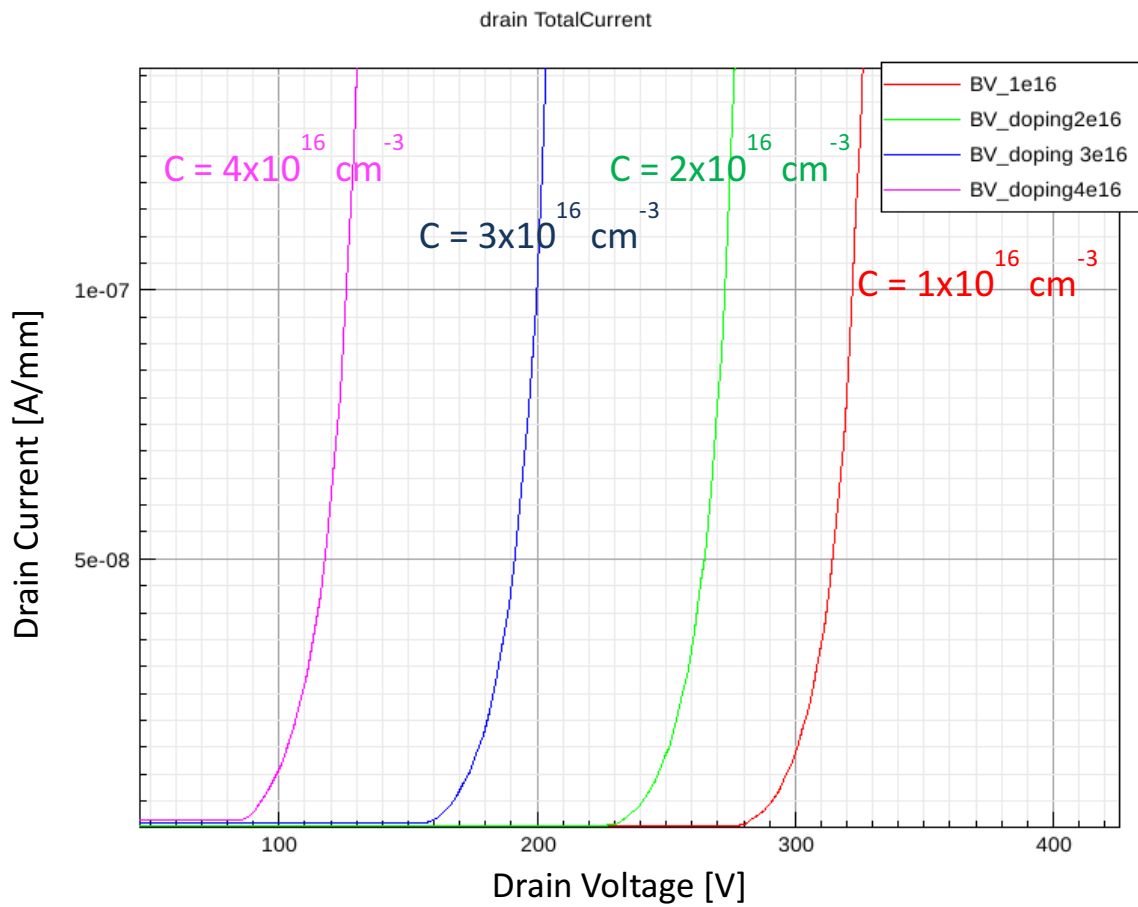
**Figure 32.** Electron impact ionization at breakdown.

The breakdown voltage has been found for the device seen in figure 27 when the channel had a carbon doping of  $4 \times 10^{16} \text{ cm}^{-3}$ . The following simulations are made in order to investigate the impact of doping concentration on breakdown voltage.

The same device is simulated four times with different channel doping varying from  $4 \times 10^{16} \text{ cm}^{-3}$  to  $1 \times 10^{16} \text{ cm}^{-3}$ . The results of  $I_{DS}/V_{DS}$  characteristics for these simulations are overlaid in figure 33. Notice that as the channel doping decreases, the breakdown voltage increases. The breakdown voltage is around 85 V when the channel doping concentration is  $4 \times 10^{16} \text{ cm}^{-3}$  and it increases up to 280 V when the channel doping concentration is  $1 \times 10^{16} \text{ cm}^{-3}$ .

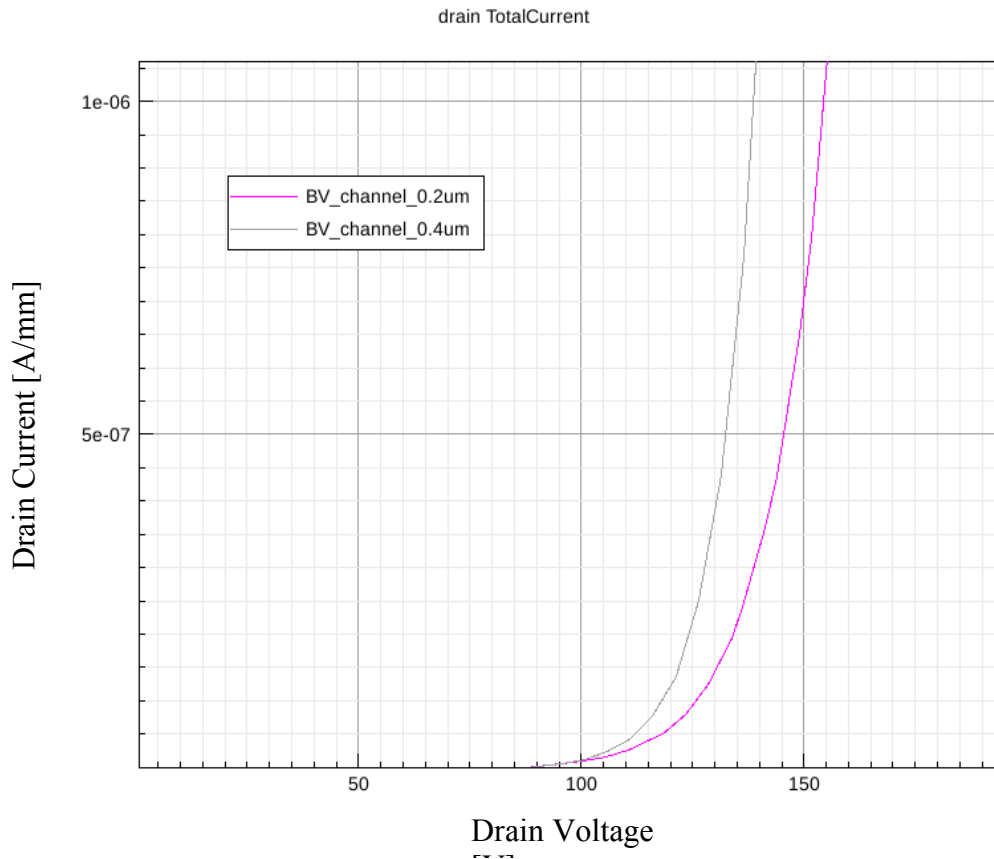
The n-type channel obtained with donor-like carbon doping will cause current leakage and decrease the breakdown voltage. From simulation results, we can see that the ideal case would be to have an undoped GaN channel. However, in reality, GaN is generally n-type as grown due to presence of impurities and vacancies. GaN-on-Si presents impurities such as silicon, oxygen and nitrogen vacancies [5]. Presence of Nitrogen vacancies in GaN can be

considered as the main cause of n-type grown GaN [19]. In order to compensate donor-like vacancies in GaN, the channel is p-type doped with acceptor-like carbon (carbon substituting for N:  $C_N$ ). The low carbon doping ( $C < 5 \times 10^{16} \text{ cm}^{-3}$ ) will form deep acceptor-like traps (C is 0.9 eV above valence band) [19]. The nitrogen vacancies in GaN channel can be simulated in TCAD as donor-like traps with an energy level of 2.6 eV above valence band.



**Figure 33.**  $I_{DS}/V_{DS}$  characteristics for different channel doping concentrations.

Another parameter that affects the breakdown voltage can be the channel length. The breakdown voltage is simulated twice for the model presented in figure 27 with a GaN channel of 0.4  $\mu\text{m}$  and 0.2  $\mu\text{m}$ , both having a channel doping concentration of  $4 \times 10^{16} \text{ cm}^{-3}$ . The nitrogen vacancies discussed previously are ignored in these simulations and the GaN channel is n-type carbon doped. The breakdown voltage simulation results for these two models are overlaid in figure 34. As it can be seen in figure 34, HEMT structure with a thicker channel length (0.4  $\mu\text{m}$ ) has a slightly smaller breakdown voltage.



**Figure 34.**  $I_{\text{DS}}/V_{\text{DS}}$  characteristics for different channel lengths.

Several papers show that having a thicker channel would improve the breakdown voltage, which is in contradiction with the simulation results above. A thick channel is suggested to reduce deep traps in the channel and reduce the electron capture probability by deep traps in the GaN buffer [20]. Therefore, buffer-related current collapse is suppressed in the thick GaN channel [20]. In my simulations, the deep traps within the channel were not simulated and the buffer was not included in the simulations. This might be the cause of wrong simulation results.



## 4 Conclusion

GaN based HEMTs are the next revolution in power electronics where high voltage, high current applications are necessary. Improving the breakdown voltage and reducing the defects in GaN HEMTs would result in more reliable GaN power amplifiers, operating at high bias conditions.

The effects of GaN channel layer doping concentration and thickness on breakdown voltage were investigated using a model structure in which only AlGaN barrier and GaN channel were present (cf. figure 27). The GaN HEMT was simulated using TCAD Sentaurus software. The simulation results suggested that lower doping of n-type GaN channel results in higher breakdown voltage. However, it is experimentally impossible to have an undoped GaN channel due to donor-like impurities. Therefore, further simulations should be done considering the donor-like traps and p-type carbon doping of GaN channel.

The comparison of breakdown voltage simulations for a thin and thick GaN channel layer suggested that having a thinner channel would increase the breakdown voltage. However, the latter is in contradiction with other research papers, which suggested that a thicker channel would reduce current-collapse and improve the breakdown voltage [20]. In order to have a more reliable simulation of GaN HEMT, the GaN buffer should be added under the GaN channel and the impurities within GaN should be considered.

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