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**Bayram et al.**

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(54) **DUAL PHASE GALLIUM NITRIDE MATERIAL FORMATION ON (100) SILICON**

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(\*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 260 days.

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*Primary Examiner* — Hsin-Yi Hsieh

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(74) *Attorney, Agent, or Firm* — Scully, Scott, Murphy & Presser, P.C.; Louis J. Percello, Esq.

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(57) **ABSTRACT**

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**H01L 29/04** (2006.01)

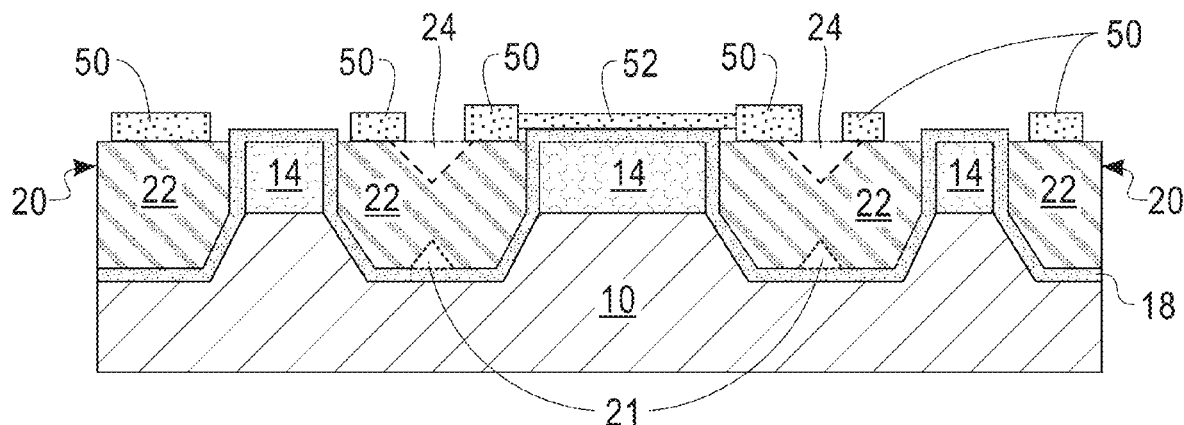
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(58) **Field of Classification Search**  
USPC ..... 438/44; 257/627, E21.112  
See application file for complete search history.

A method for selective formation of a dual phase gallium nitride material on a (100) silicon substrate. The method includes forming a blanket layer of dielectric material on a surface of a (100) silicon substrate. The blanket layer of dielectric material is then patterned forming a plurality of patterned dielectric material structures on silicon substrate. An etch is employed that selectively removes exposed portions of the silicon substrate. The etch forms openings within the silicon substrate that expose a surface of the silicon substrate having a (111) crystal plane. A contiguous AlN buffer layer is then formed on exposed surfaces of each patterned dielectric material structure and on exposed surfaces of the silicon substrate. A dual phase gallium nitride material is then formed on a portion of the contiguous AlN buffer layer and surrounding each sidewall of each patterned dielectric material structure.

**13 Claims, 8 Drawing Sheets**



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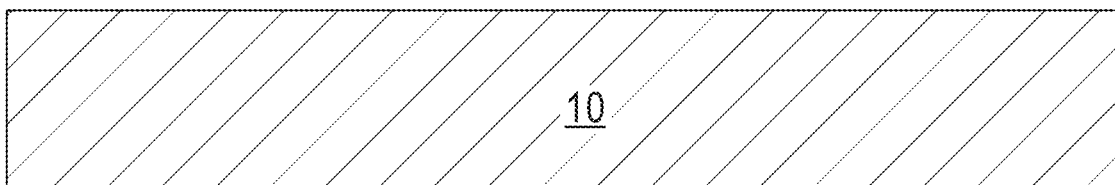


FIG. 1

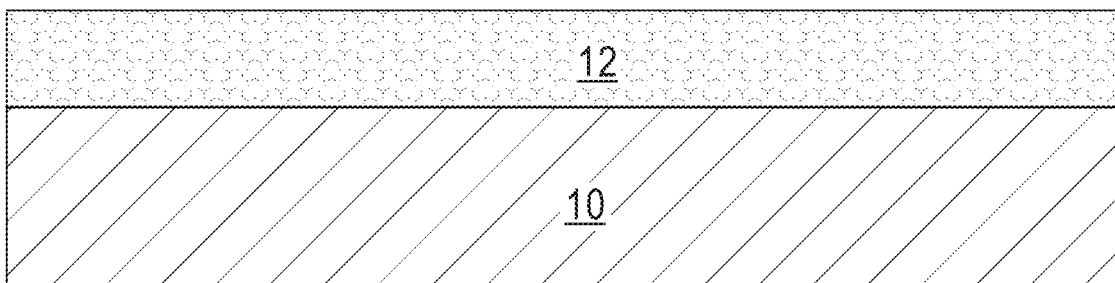


FIG. 2

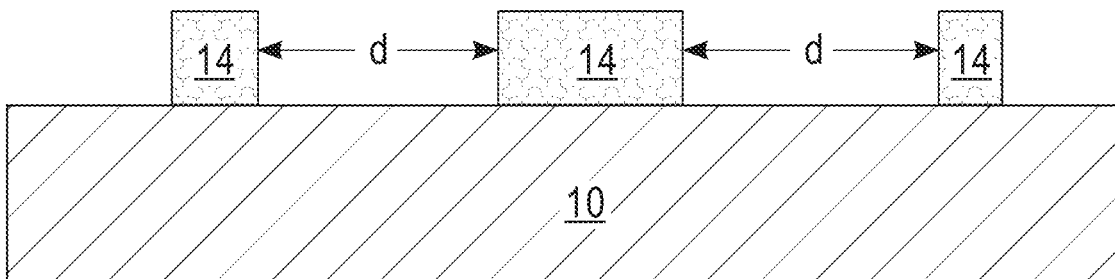


FIG. 3

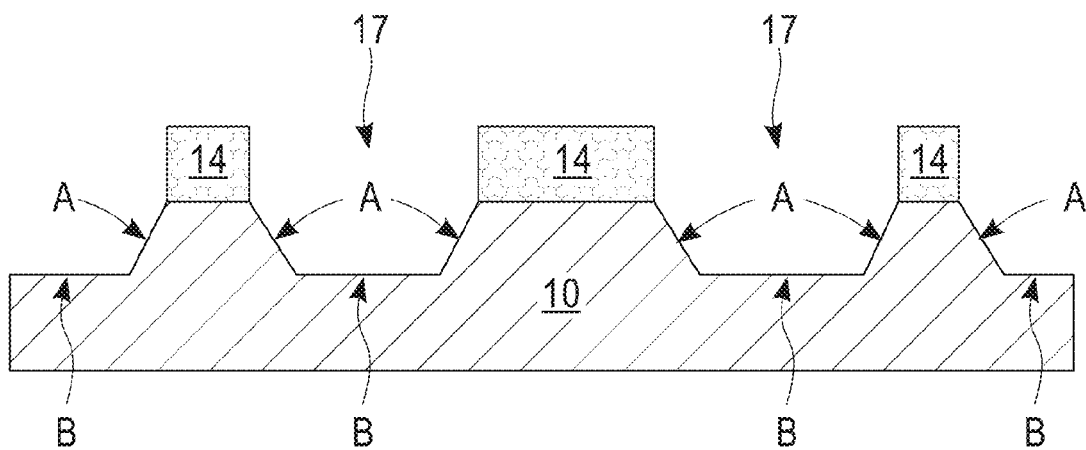


FIG. 4

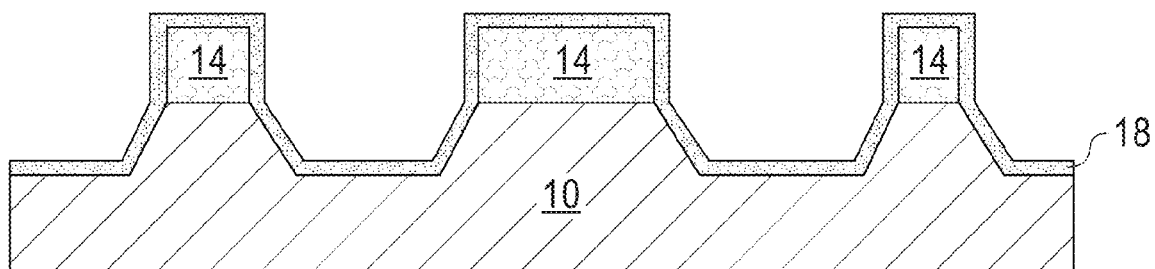


FIG. 5

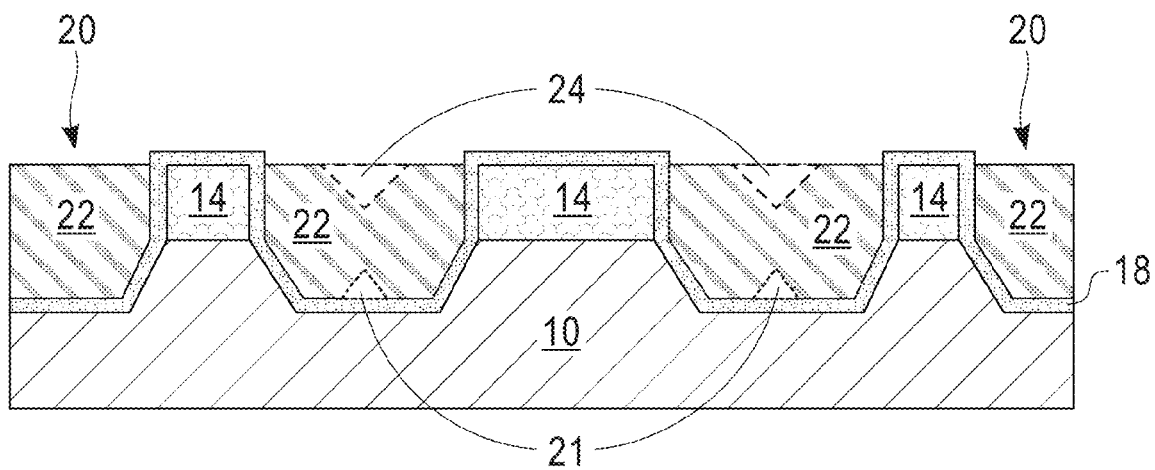


FIG. 6

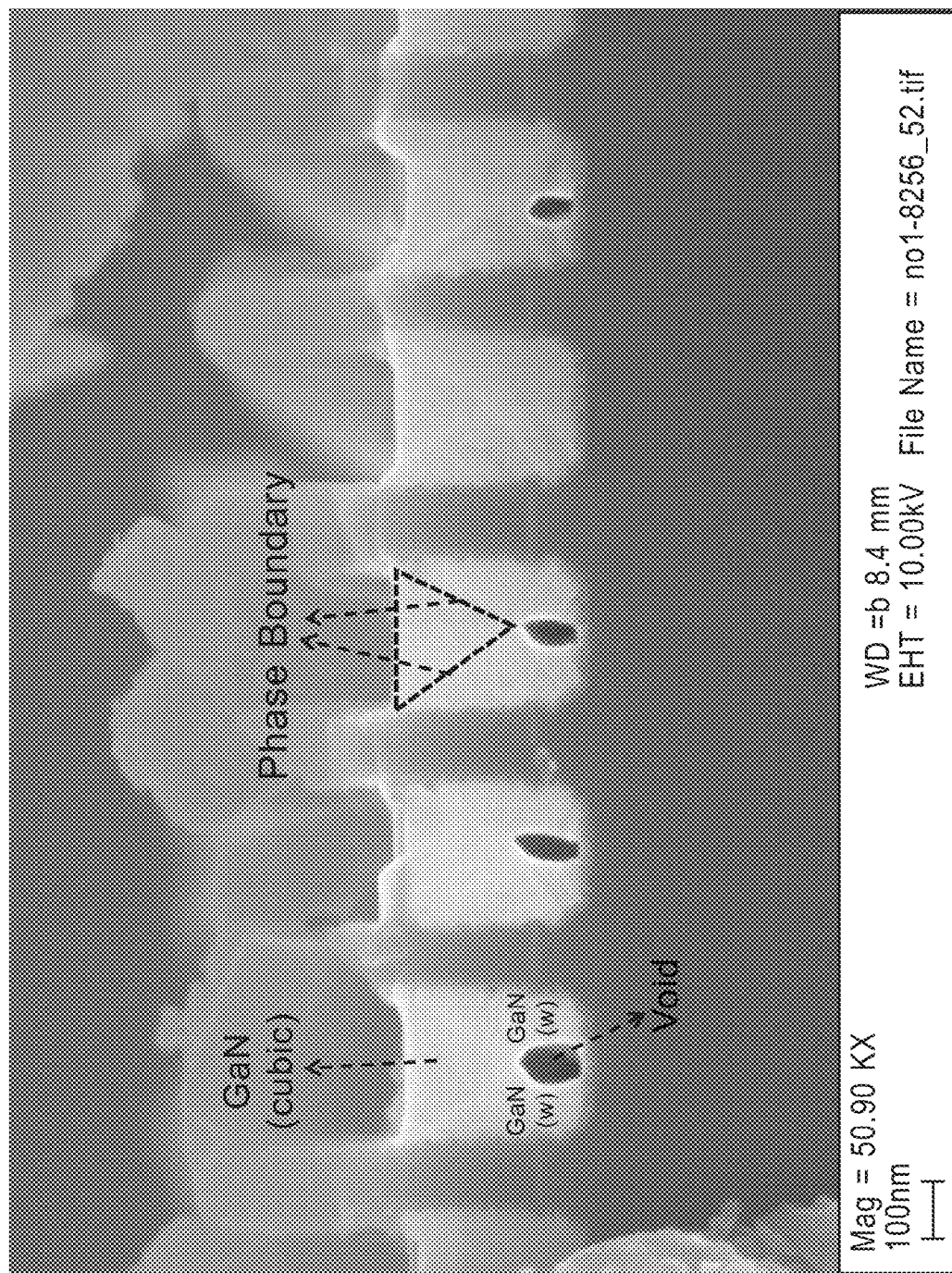


FIG. 7

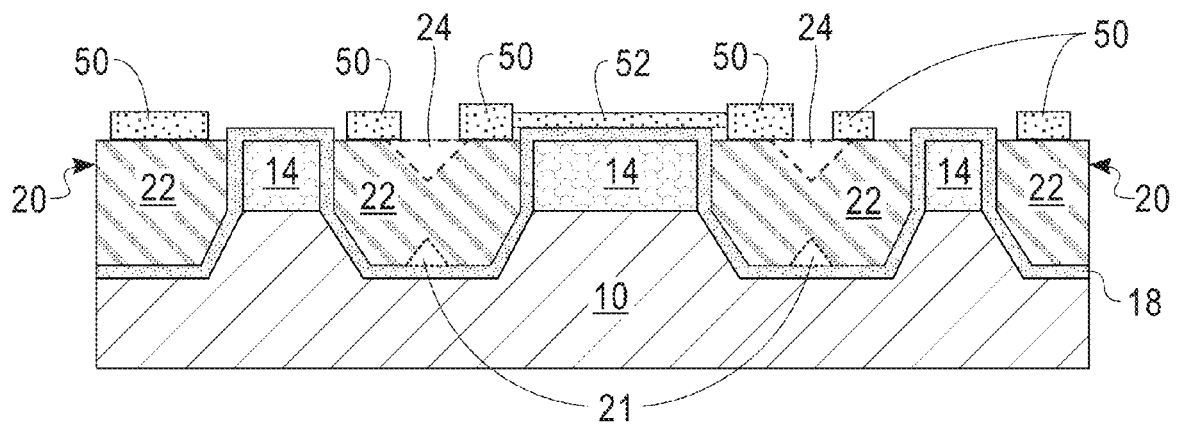


FIG. 8

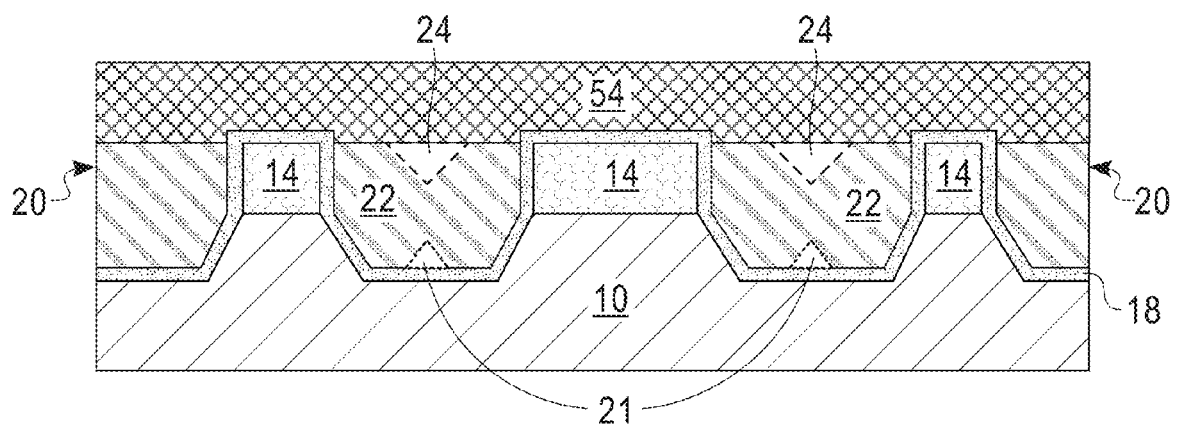


FIG. 9

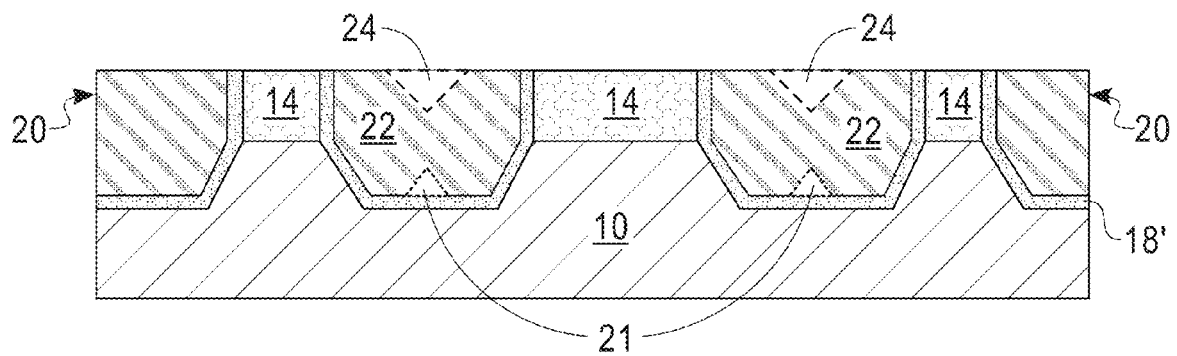
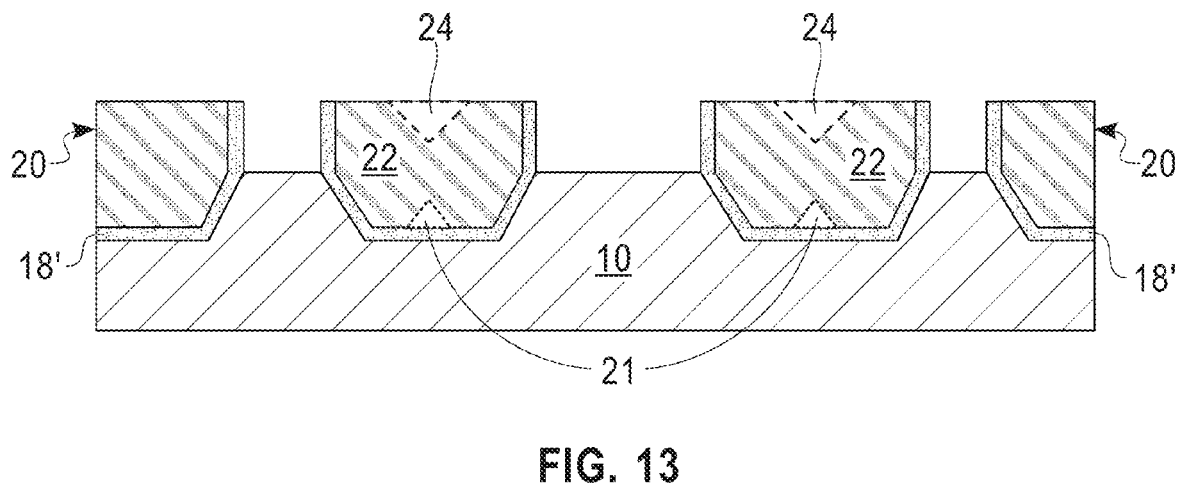
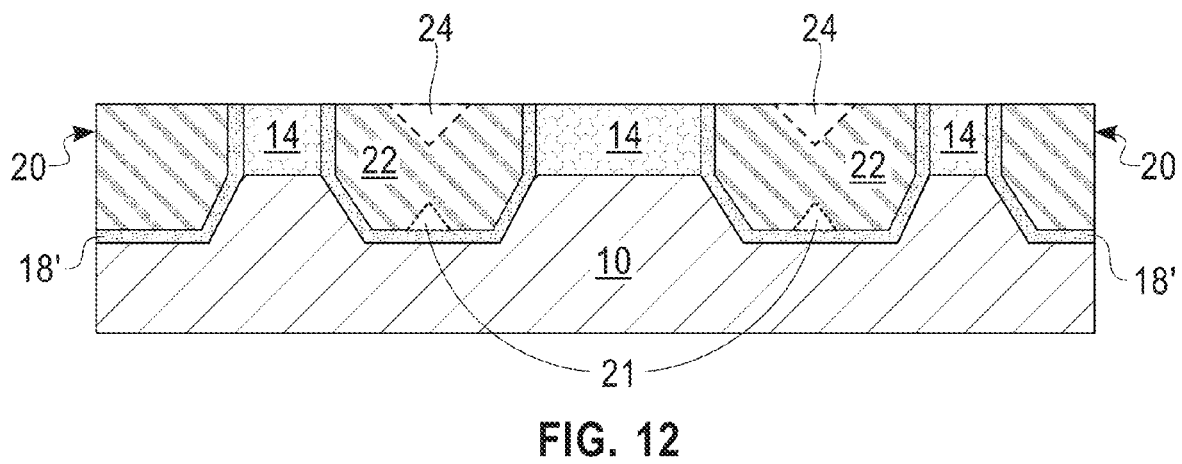
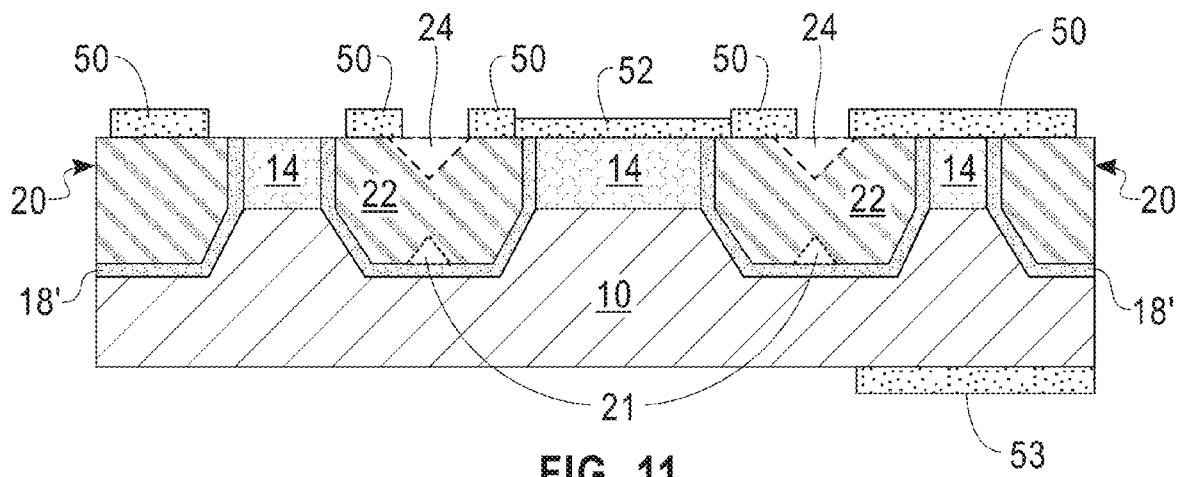


FIG. 10



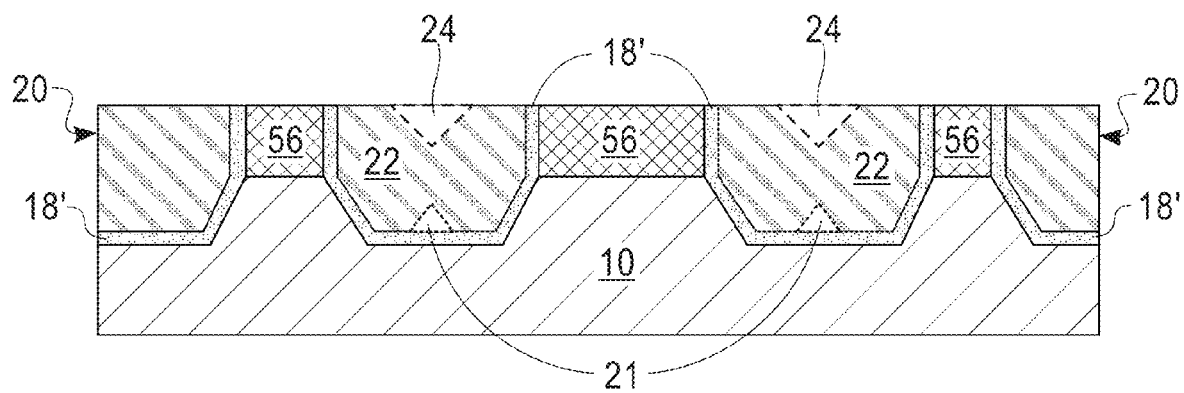


FIG. 14

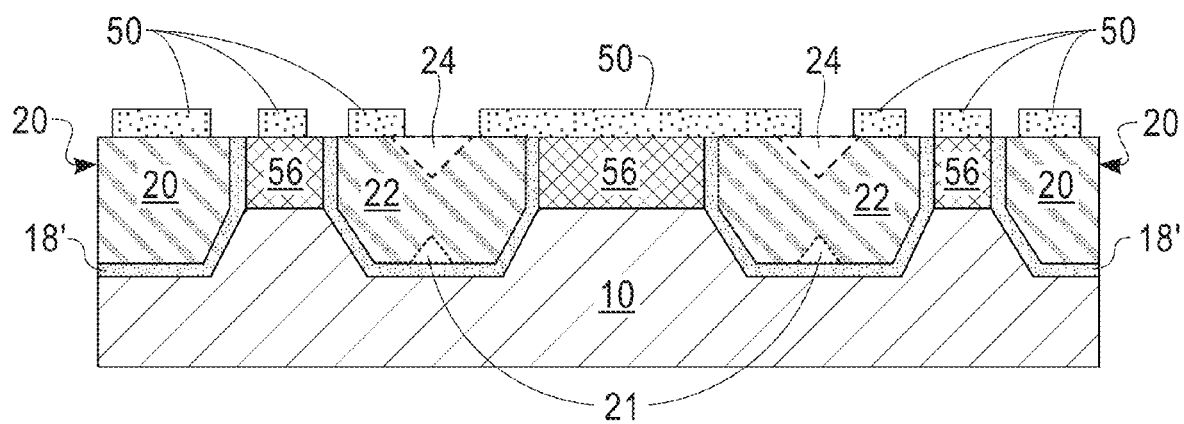


FIG. 15

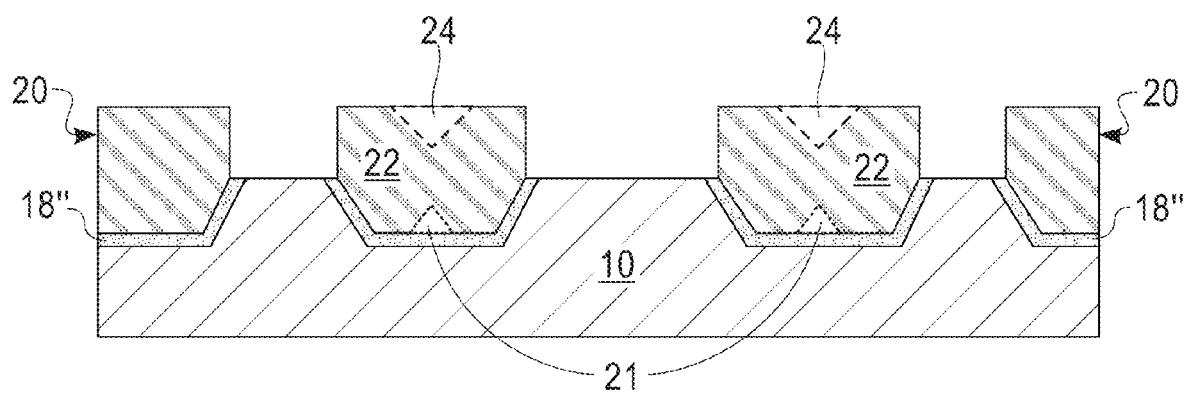


FIG. 16



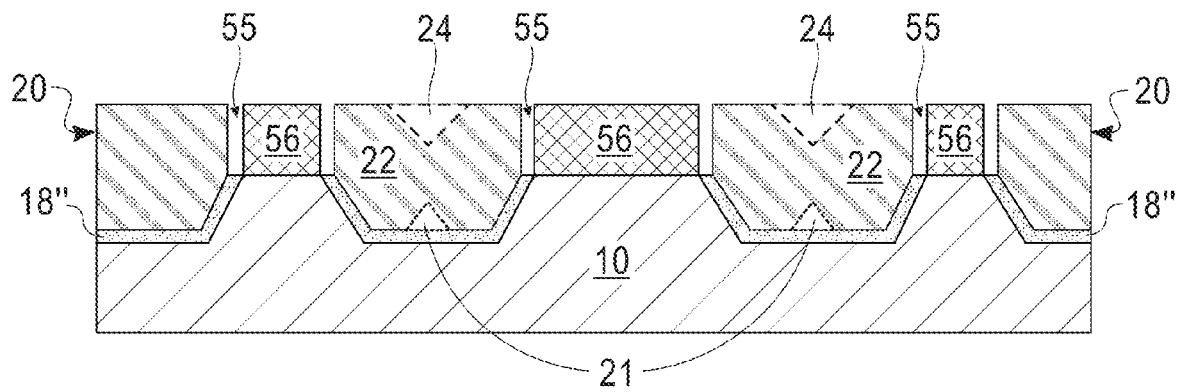


FIG. 17

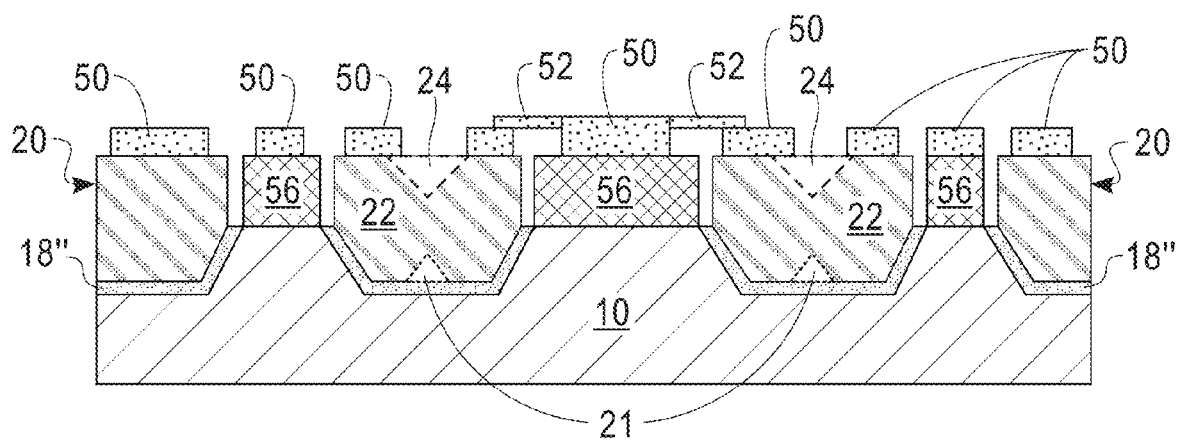


FIG. 18

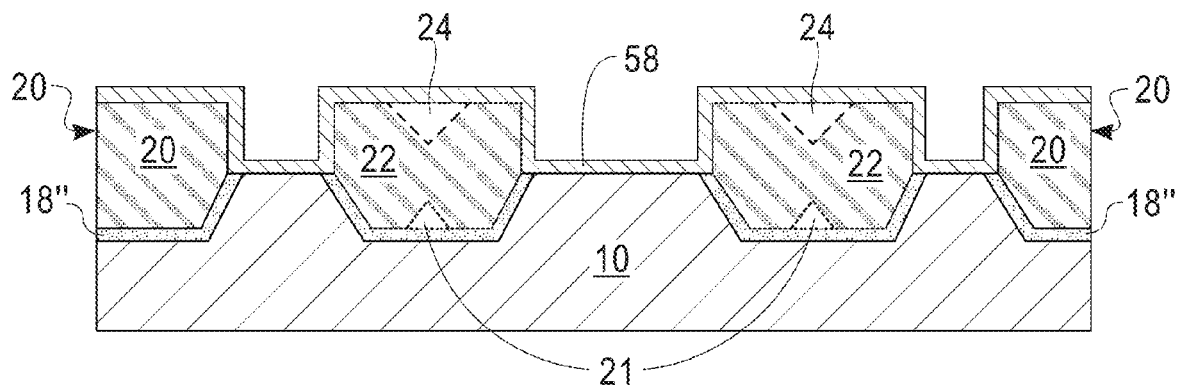


FIG. 19

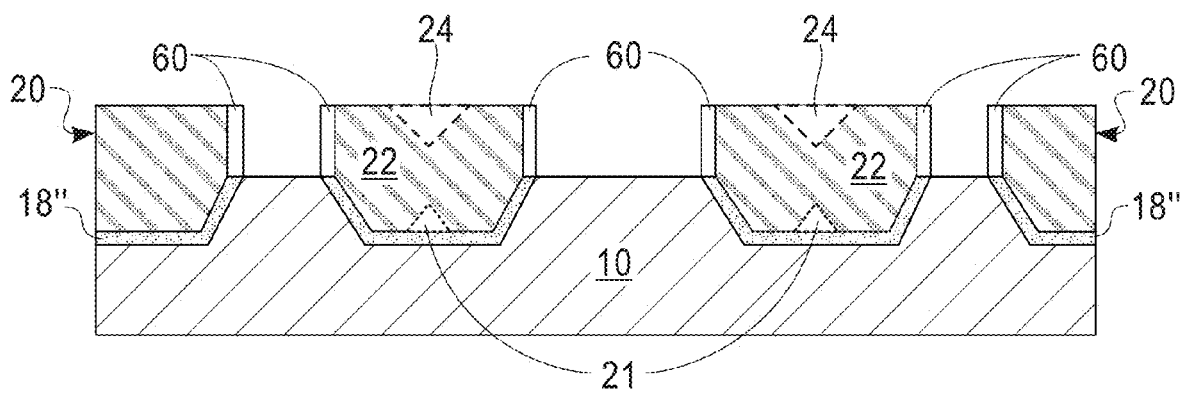


FIG. 20

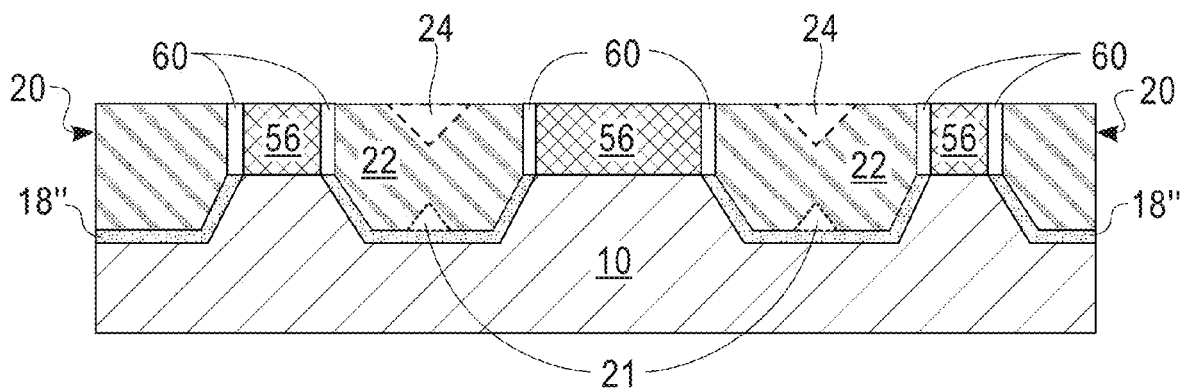


FIG. 21

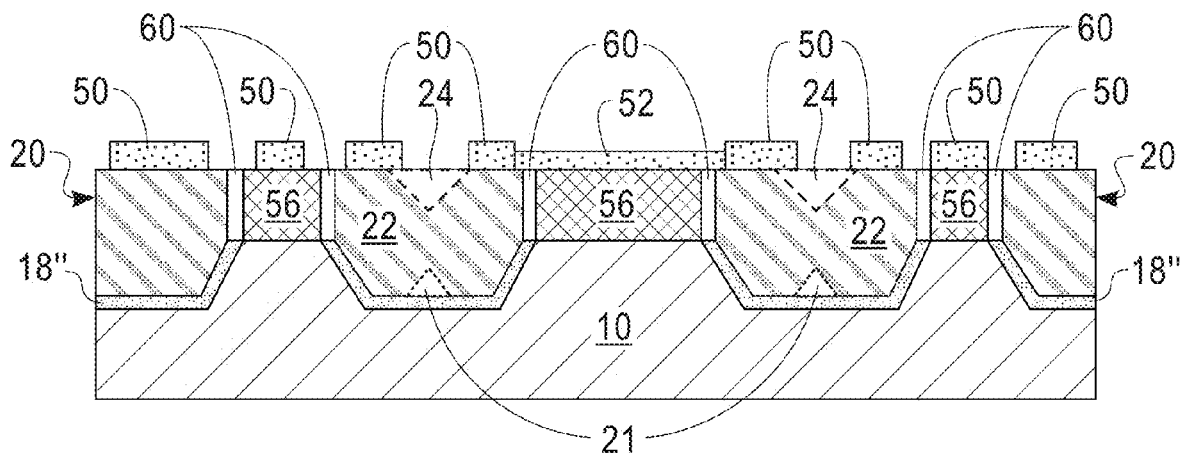


FIG. 22

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## DUAL PHASE GALLIUM NITRIDE MATERIAL FORMATION ON (100) SILICON

### BACKGROUND

The present disclosure generally relates to a method for integrating Group III nitrides (e.g., GaAlInN) with silicon and more particularly to a method of selectively forming a dual phase gallium nitride material on a (100) silicon substrate. The present disclosure also relates to a semiconductor structure including a dual phase gallium nitride material surrounding sidewalls of a patterned dielectric material structure and located adjacent a surface of the (100) silicon substrate having a (111) crystal plane.

Group III nitride materials are a unique group of semiconductor materials which can be used in a wide variety of applications including, for example, optoelectronics, photovoltaics and lighting. Group III nitride materials are composed of nitrogen and at least one element from Group III, i.e., aluminum (Al), gallium (Ga) and indium (In), of the Periodic Table of Elements. Illustrative examples of some common gallium nitrides are GaN, GaAlN, and GaAlInN. By changing the composition of Al, Ga and/or In within a Group III nitride material, the Group III nitride material can be tuned along the electromagnetic spectrum; mainly from 210 nm to 1770 nm. This spectrum includes the visible light emitting diode (LED), which is more than a 10 billion dollar industry with a forecasted double digit yearly growth rate. This continuous growth in LED demand enables the infrastructural build-up for the growth and fabrication of Group III nitride based semiconductor devices.

One of the bottlenecks for Group III nitride based semiconductor devices is a lack of a latticed matched substrate. Some of the conventional substrates are sapphire ( $\text{Al}_2\text{O}_3$ ), silicon carbide (SiC), silicon (Si), and zinc oxide (ZnO) that have about 13%, 3%, 17% and 2%, respectively, lattice mismatch with GaN. Currently, lattice matched freestanding GaN and AlN substrates are being developed. However, lattice matched substrates suffer from availability and cost.

Most of the Group III nitride consumer-targeted devices are conventionally grown on sapphire substrates. There is, however, a need for the development of Group III nitride technology on more available and cheaper substrates such as silicon. The integration between Group III nitrides and silicon substrates are difficult because of the different crystal structure and lattice constant of those materials. As such, a method is needed which can be used to easily integrate Group III nitride materials with silicon substrates.

### SUMMARY

In one aspect of the present disclosure, a method for selectively forming a dual phase gallium nitride material on a silicon substrate is provided. The method of the present disclosure includes first forming a blanket layer of dielectric material on an uppermost surface of a (100) silicon substrate. Next, the blanket layer of dielectric material is patterned forming a plurality of patterned dielectric material structures on portions of the uppermost surface of the (100) silicon substrate and exposing other portions of the uppermost surface of the (100) silicon substrate. The exposed other portions of the uppermost surface of the (100) silicon substrate are then etched to expose a surface within the (100) silicon substrate having a (111) crystal plane. A contiguous AlN buffer layer is then formed on exposed surfaces of each patterned dielectric material structure and on exposed surfaces of the silicon substrate. A dual phase gallium nitride material is then

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formed on a portion of the contiguous AlN buffer layer and surrounding each sidewall of each patterned dielectric material structure. In accordance with the present disclosure, the dual phase gallium nitride material comprises a wurtzite phase and a cubic phase, wherein the cubic phase defines at least a portion of an uppermost surface of the gallium nitride material.

In another aspect of the present disclosure, a semiconductor structure is provided. The semiconductor structure of the present disclosure includes a (100) silicon substrate having a plurality of patterned dielectric material structures located on an uppermost surface of the silicon substrate and a plurality of openings located within the silicon substrate and beneath the plurality of patterned dielectric material structures, wherein each opening exposes a surface of the silicon substrate having a (111) crystal plane. The structure of the present disclosure further includes a dual phase gallium nitride material surrounding each sidewall of each patterned dielectric material structure and located adjacent to the surface of the silicon substrate having the (111) crystal plane. In accordance with the present disclosure, the dual phase gallium nitride material comprises a wurtzite phase and a cubic phase, wherein the cubic phase defines at least a portion of an uppermost surface of the gallium nitride material. A semiconductor device can be positioned upon and within the gallium nitride material.

In a further aspect of the present disclosure, a semiconductor structure is provided that includes a (100) silicon substrate having a plurality openings located within the silicon substrate, wherein each opening exposes a surface of the silicon substrate having a (111) crystal plane. This structure further includes an epitaxial semiconductor material located on an uppermost surface of the (100) silicon substrate, and a dual phase gallium nitride material located adjacent to the surface of the silicon substrate having the (111) crystal plane and adjacent a portion of the epitaxial semiconductor material. In accordance with the present disclosure, the dual phase gallium nitride material comprises a wurtzite phase and a cubic phase, wherein the cubic phase defines at least a portion of an uppermost surface of the gallium nitride material. The structure also includes at least one semiconductor device located upon and within the dual phase gallium nitride material and at least one other semiconductor device located upon and within the epitaxial semiconductor material.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a pictorial representation (through a cross sectional view) illustrating a (100) silicon substrate that can be employed in one embodiment of the present disclosure.

FIG. 2 is a pictorial representation (through a cross sectional view) illustrating the silicon substrate of FIG. 1 after forming a blanket layer of dielectric material on an uppermost surface of the silicon substrate.

FIG. 3 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 2 after forming patterned dielectric material structures from the blanket layer of dielectric material.

FIG. 4 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 3 after etching exposed surfaces of the silicon substrate to form openings in the silicon substrate that expose a surface of the silicon substrate having a (111) crystal plane.

FIG. 5 is a pictorial representation (through a cross sectional view) of the structure of FIG. 4 after forming a contiguous AlN buffer layer on exposed surfaces of each patterned dielectric material structure and on exposed surfaces of the silicon substrate within each opening.

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FIG. 6 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 5 after forming a dual phase gallium nitride material on a portion of the contiguous AlN buffer layer and surrounding each sidewall of each patterned dielectric material structure.

FIG. 7 is a scanning electron micrograph (SEM) of a structure including a dual phase gallium nitride material integrated on a (100) silicon substrate that is formed using the method of the present disclosure.

FIG. 8 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 6 after semiconductor device fabrication.

FIG. 9 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 6 after formation of another dielectric material.

FIG. 10 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 9 after planarization which provides a planar structure.

FIG. 11 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 10 after semiconductor device fabrication.

FIG. 12 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 6 after removing an uppermost portion of the contiguous AlN buffer layer that lies atop each patterned dielectric material structure.

FIG. 13 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 12 after removing each patterned dielectric material structure.

FIG. 14 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 13 after epitaxially growth of a semiconductor material on an exposed portion of the uppermost surface of the (100) silicon substrate and planarization.

FIG. 15 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 14 after semiconductor device fabrication.

FIG. 16 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 13 after removing sidewall portions of the remaining AlN buffer layer.

FIG. 17 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 16 after epitaxially growth of a semiconductor material on an exposed portion of the uppermost surface of the (100) silicon substrate and planarization.

FIG. 18 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 17 after device fabrication.

FIG. 19 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 16 after forming a dielectric material liner.

FIG. 20 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 19 after removing portions of the dielectric material liner and forming dielectric spacers.

FIG. 21 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 20 after epitaxially growth of a semiconductor material on an exposed portion of the uppermost surface of the (100) silicon substrate and planarization.

FIG. 22 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 21 after semiconductor device fabrication.

#### DETAILED DESCRIPTION

The present disclosure, which provides a method of selectively forming a dual phase gallium nitride material on a (100)

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silicon substrate, and a semiconductor structure including a dual phase gallium nitride material surrounding sidewalls of a patterned dielectric material structure and present on a (111) crystal plane of a (100) silicon substrate, will now be described in greater detail by referring to the following discussion and drawings that accompany the present disclosure. It is noted that the drawings are provided for illustrative purposes only and are not drawn to scale.

In the following description, numerous specific details are set forth, such as particular structures, components, materials, dimensions, processing steps and techniques, in order to illustrate the present disclosure. However, it will be appreciated by one of ordinary skill in the art that various embodiments of the present disclosure may be practiced without these, or with other, specific details. In other instances, well-known structures or processing steps have not been described in detail in order to avoid obscuring the various embodiments of the present disclosure.

It will be understood that when an element as a layer, region or substrate is referred to as being “on” or “over” another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being “directly on” or “directly over” another element, there are no intervening elements present. It will also be understood that when an element is referred to as being “connected” or “coupled” to another element, it can be directly connected or coupled to the other element or intervening elements may be present. In contrast, when an element is referred to as being “directly connected” or “directly coupled” to another element, there are no intervening elements present.

Metalorganic chemical vapor deposition (MOCVD) has been the backbone of the Group III-nitrides growth and an industry standard for epitaxial growth of compound semiconductors on a crystalline substrate. There has been a sustained improvement in wafer throughput by MOCVD making it cost-effective in mass-production. For GaN-based transistors to be competitive: epitaxial process and substrate cost must be <\$2/cm<sup>2</sup> as well as current power device material demand (>10<sup>7</sup> 6-inch wafers per year) must be fulfilled through mature process platform.

MOCVD technology is the most mature and scalable to volume production. All commercial electronics have so far been produced with MOCVD systems (especially LED). Silicon substrates are the most scalable and cost effective for volume production. Adequate epitaxial film uniformity, defect levels, device reliability and process cost structure must be achieved to permit the use of gallium nitride (GaN) on Si based devices to achieve widespread use in power electronics. Device processing should be CMOS compatible to achieve commercially viability. Thus, there is a need for the integration of GaN devices on silicon substrates that benefits the MOCVD growth capabilities. Particularly, silicon (100) is of interest due to integration of GaN-based devices with CMOS technology.

Currently, for the MOCVD growth of GaN onto silicon substrates, silicon (111) substrates are employed. Si (111) is preferred for GaN epitaxy due to the three fold symmetry of Si 111 plane and hexagonal structure (six-fold symmetry) of GaN. Si (100) is another substrate of interest due to possible integration of GaN devices with Si (i.e., CMOS) electronics. However, GaN on Si (001) leads to polycrystalline structures or very rough surfaces consisting of many grains. The reason for this is the fourfold symmetry and the possibility for GaN with its sixfold symmetry to grow with two preferred rotational alignments on this surface. For such c-axis oriented material, the lattice mismatch is anisotropic and yields

approximately 15% for  $\langle 112\text{bar}0 \rangle \parallel \langle \text{Si} \langle 1\text{bar}00 \rangle$  and 0.7% for  $\langle 101\text{bar}0 \rangle \parallel \langle \text{Si} \langle 1\text{bar}00 \rangle$ . While these mismatch values are lower than for Si (111), the material quality is low due to twist boundaries. Thus, off cut-oriented Si (100) substrates (typically  $4^\circ$  to  $7^\circ$  towards (110)) are preferred for single crystalline GaN epitaxy. However, for true integration with silicon electronics, it is essential to develop GaN epitaxy on non-off cut Si (100) substrates as off cut substrates lead to anisotropy and performance issue in silicon electronic devices.

Although the lattice mismatch between (0001) GaN and (111) Si is  $-16.8\%$ , the main bottleneck for GaN-on-Silicon epitaxy is the thermal lattice mismatch (approximately  $-53\%$ ) that leads to cracking. The present disclosure provides a method to reconcile the issue of lattice and thermal mismatch of the direct epitaxy growth and thus allow for facile integration of a gallium nitride material and a (100) silicon material. The term "gallium nitride material" as used throughout the present disclosure denotes pure gallium nitride, or gallium nitride that may include other Group III elements such as, for example, Al and/or In. As such, the term "gallium nitride material" as used throughout the present disclosure includes gallium nitride-containing materials such as, for example, GaN, GaAlN, GaInN and GaAlInN.

The conventional phase of gallium nitride materials is typically wurtzite, which is not a preferred phase for photonic devices. For example, GaN wurtzite to cubic transition can be particularly beneficial for light emitting diodes as the cubic phase is non-polar. The cubic phase of GaN eliminates piezoelectric fields and enhances radiative recombination dynamics. The method of the present disclosure also provides a dual phase gallium nitride material which has two distinct phases, a wurtzite phase and a cubic phase, wherein the cubic phase defines at least a portion of an uppermost surface of the gallium nitride material.

The method of the present disclosure includes forming a blanket layer of dielectric material on a surface of a (100) silicon substrate. The blanket layer of dielectric material is then patterned forming a plurality of patterned dielectric material structures on the silicon substrate. An etch is employed that selectively removes exposed portions of the silicon substrate. The etch forms openings within the silicon substrate that expose a surface of the silicon substrate having a (111) crystal plane. A contiguous AlN buffer layer is then formed on exposed surfaces of each patterned dielectric material structure and on exposed surfaces of the silicon substrate. A dual phase gallium nitride material is then formed on a portion of the contiguous AlN buffer layer and surrounding each sidewall of each patterned dielectric material structure. The dual phase gallium nitride material that is provided comprises a wurtzite phase and a cubic phase, wherein the cubic phase defines at least a portion of an uppermost surface of the gallium nitride material. This method will now be described in greater detail by referring to FIGS. 1-6.

Referring first to FIG. 1, there is illustrated a silicon substrate **10** which has a (100) crystallographic surface orientation that can be employed in one embodiment of the present disclosure. The silicon substrate **10** having the (100) crystallographic surface orientation may also be referred to herein as "a (100) silicon substrate". In one embodiment, and as illustrated in the drawings, the (100) silicon substrate **10** may be a bulk semiconductor material having silicon located between a planar uppermost surface and a planar bottommost surface. In another embodiment, the (100) silicon substrate **10** may be a topmost layer of a silicon-on-insulator substrate. In such an embodiment, an insulator material such as, for example, a dielectric material, can be located between the planar uppermost surface and a planar bottommost surface of the silicon-

on-insulator substrate, and the (100) silicon substrate **10** is located on an uppermost surface of the insulator material. A semiconductor material such as, for example, silicon, germanium, silicon germanium, a III-V compound semiconductor material or a II-V semiconductor material can be located beneath the insulator material of the silicon-on-insulator substrate. In yet another embodiment, the (100) silicon substrate **10** can be a topmost layer of a multilayered stack of semiconductor materials. In still yet another embodiment, the (100) silicon substrate can be a topmost layer of a silicon-on-sapphire substrate.

The (100) silicon substrate **10** that can be employed in the present disclosure is typically a single crystalline material and may be doped, undoped or contain regions that are doped and other regions that are non-doped. The dopant may be an n-type dopant selected from an Element from Group VA of the Periodic Table of Elements (i.e., P, As and/or Sb) or a p-type dopant selected from an Element from Group IIIA of the Periodic Table of Elements (i.e., B, Al, Ga and/or In). The (100) silicon substrate **10** may contain one region that is doped with a p-type dopant and other region that is doped with an n-type dopant. The thickness of the (100) silicon substrate **10** can be from 50 microns to 2 cm, although lesser and greater thickness can also be employed.

Referring now to FIG. 2, there is illustrated the (100) silicon substrate **10** of FIG. 1 after forming a blanket layer of dielectric material **12** on an uppermost surface of the (100) silicon substrate **10**. As shown, the blanket layer of dielectric material **12** is a contiguous layer that covers the entire uppermost surface of the (100) silicon substrate **10**. In some embodiments, the blanket layer of dielectric material **12** can be comprised of silicon dioxide, silicon nitride, or silicon oxynitride.

In one embodiment of the present disclosure, the blanket layer of dielectric material **12** can be formed using a thermal process including, for example, thermal oxidation, thermal nitridation and thermal oxynitridation. In such an embodiment, the (100) silicon substrate **10** is heated in an oxidizing and/or nitriding ambient at a temperature of  $700^\circ\text{C}$ . or greater. In another embodiment of the present disclosure, the blanket layer of dielectric material **12** can be formed onto the uppermost surface of the (100) silicon substrate **10** by utilizing a deposition process such as, for example, chemical vapor deposition, and plasma enhanced chemical vapor deposition. Notwithstanding which technique is used in forming the blanket layer of dielectric material **12**, the blanket layer of dielectric material **12** typically has a thickness a few monolayers to as thick as a couple of microns or more.

Referring to FIG. 3, there is illustrated the structure of FIG. 2 after forming a plurality of patterned dielectric material structures (hereinafter patterned dielectric material structures **14**) from the blanket layer of dielectric material **12**. As shown, the patterned dielectric material structures **14** are located on portions of the uppermost surface of the (100) silicon substrate **10**, while other portions of the (100) silicon substrate are exposed.

In one embodiment, of the present disclosure, a distance,  $d$ , from a sidewall surface of one patterned dielectric material structure to a sidewall surface of a neighboring patterned dielectric material structure is from 200 nm to 500 nm. A distance within the range from 200 nm to 500 nm can be referred to herein as a short distance. In another embodiment of the present disclosure, a distance,  $d$ , from a sidewall surface of one patterned dielectric material structure to a sidewall surface of a neighboring patterned dielectric material structure may be greater than 500 nm up to 5000 nm. A distance within the range of greater than 500 nm up to 5000

nm may be referred to herein as a long distance. In some embodiments of the present disclosure, a shorter distance is preferred over a longer distance since the surface coverage of the cubic phase of the dual phase gallium nitride material (to be subsequently formed) increases with the shorter distances. The patterned dielectric material structures **14** are employed in the present disclosure as an etch mask and are used in forming periodic openings within the (100) silicon substrate **10**. In the case of longer distances, if the growth fronts of the wurtzite phase of the gallium nitride material meet, a cubic phase will form. However, in this instance the quality and control over the cubic phase material will be reduced for the longer distances.

The patterned dielectric material structures **14** can be formed by lithography and etching. The lithographic step used in forming the patterned dielectric material structures **14** includes applying a blanket layer of a photoresist material on the uppermost surface of the blanket layer of dielectric material, exposing the photoresist material to radiation and developing the exposed photoresist material. The etching step used in forming the patterned dielectric material structures **14** may include a dry etching process or a chemical wet etching process. When a dry etching process is employed, one of reactive ion etching, plasma etching, and ion beam etching can be used. When a chemical wet etch process is employed, a chemical etchant that selectively removes exposed portions of the blanket layer of dielectric material is used. After the etching process has been performed, the patterned photoresist material is stripped from the structure utilizing a conventional resist stripping process such as, for example, ashing.

Each patterned dielectric material structure **14** that is formed has four sides, i.e., four vertical sidewalls, and thus is in the shape of a parallelogram. In one embodiment, each patterned dielectric material structure **14** is a square. In another embodiment, each patterned dielectric material structure **14** is a rectangle.

Each patterned dielectric material structure **14** has a length and width. In some embodiments, the length can equal the width. In other embodiments, the length can be different (greater than or less than) from the width. The length of each patterned dielectric material structure **14** can be within a range from 10 nm to 100  $\mu$ m, while the width can be from 10 nm to 100  $\mu$ m. Other width and length values are possible with the upper limit being application dependent. In the present application, the width of each patterned dielectric material structure **14** runs parallel to the cross section shown in FIG. 3, while the length of each patterned dielectric material structure **14** runs into and out of the cross section shown in FIG. 3.

Referring now to FIG. 4, there is illustrated the structure of FIG. 3 after etching exposed surfaces of the (100) silicon substrate **10** using each patterned dielectric material structures **14** as an etch mask to form openings **17** in the (100) silicon substrate **10** that expose a surface (designated as "A" in FIG. 4) of the (100) silicon substrate **10** within each opening **17** that has a (111) crystal plane. By "(111) crystal plane" it is meant any plane within the (111) crystal plane family including, but not limited to, 111, 1 $\bar{1}$ 1, and 11 $\bar{1}$ . In the drawing, the designation "B" denotes a planar surface of the (100) silicon substrate **10** that has a (100) crystal plane which is located beneath the uppermost surface of the (100) silicon substrate **10**. By "(100) crystal plane" it is meant any plane within the (100) crystal plane family.

The etching of the exposed surfaces of the (100) silicon substrate can be performed utilizing a crystallographic wet etch; the crystallographic wet etch may also be referred to as an anisotropic wet etch that is orientation dependent. In one

embodiment of the present disclosure, the crystallographic wet etch that is employed includes using KOH as a chemical etchant. Other chemical etchants can be used in the crystallographic wet etch as long as the chemical etchant that is selected is capable of exposing a surface of the (100) silicon substrate **10** having the (111) crystal plane. Examples of other chemical etchants that can be used in the crystallographic wet etch of the present disclosure, include, but are not limited to, an aqueous solution of ethylene diamine and pyrocatechol or tetramethylammonium hydroxide.

In accordance with an aspect of the present disclosure, each opening **17** that is formed within the (100) silicon substrate **10** has an upper portion having a width (w1) that is larger than a width (w2) of a lower portion. In some embodiments of the present disclosure, the width (w1) of the upper portion of each opening **17** is substantially the same as the distance between a sidewall surface of one patterned dielectric material structure to a sidewall surface of a neighboring patterned dielectric material, while the width (w2) of the lower portion of each opening **17** is less than w1. In one example, the width w1 is from 200 nm to 500 nm. In another example, the width w1 is greater than 500 nm up to 5000 nm. In some embodiments, an upper portion of each opening **17** can extend beneath each of the patterned dielectric material structures **16**. The depth of each opening **17** that is formed, as measured from the uppermost surface of the (100) silicon substrate **10** to surface B is from a couple nanometers to 0.7 $\times$ width of the opening.

The structure that is shown in FIG. 4 is then heated in a hydrogen atmosphere and then a prealuminumization process is performed which stabilizes the surfaces of the silicon substrate. These steps are performed prior to forming the AlN buffer layer, and prior to forming the dual phase gallium nitride material. The heating of the structure shown in FIG. 4 in a hydrogen atmosphere includes placing the structure shown in FIG. 4 into a reactor chamber of a metalorganic chemical vapor deposition (MOCVD) apparatus. In some embodiments, and prior to placing the structure shown in FIG. 4 into the MOCVD reactor chamber, the structure can be cleaned using an HF cleaning process. The MOCVD reactor chamber including the structure shown in FIG. 4 is then evacuated to a pressure of about 50-100 mbar or less and then a hydrogen atmosphere is introduced into the reactor chamber. In some embodiments, the pressure within the MOCVD reactor is at atmospheric, i.e., 760 mbar. The hydrogen atmosphere may include pure hydrogen or hydrogen admixed with an inert carrier gas such as, for example, helium and/or argon. When an admixture is employed, hydrogen comprises at least 25% or greater of the admixture, the remainder of the admixture (up to 100%) is comprised of the inert carrier gas. With the hydrogen atmosphere present in the reactor chamber, the structure is heated to a temperature of about 900° C. or less. In one embodiment, the temperature in which the structure shown in FIG. 4 is heated under the hydrogen atmosphere is from 500° C. to 600° C. In another embodiment, the temperature in which the structure shown in FIG. 4 is heated under the hydrogen atmosphere is from 600° C. to 900° C. Notwithstanding the temperature in which the structure of FIG. 4 is heated under the hydrogen atmosphere, the heating is performed for a time period of 5 minutes to 20 minutes. This step of the present disclosure is believed to clean the surfaces and hydrogenate the exposed surfaces of the (100) silicon substrate. In some embodiments, the heating under hydrogen can be replaced with heating under an inert gas.

Since gallium will react directly with silicon, a prealuminumization step is performed to stabilize the silicon nucleation sites prior to forming the dual phase gallium nitride material; no Al layer is formed during this step of the present disclosure.

sure. If the prealuminization step is not performed, a dual phase gallium nitride material will not be as selectively deposited around the patterned dielectric material structures. The prealuminization step is performed by introducing an organoaluminum precursor such as, for example, a trialkylaluminum compound, wherein the alkyl contains from 1 to 6 carbon atoms, into the reactor chamber. Examples of trialkylaluminum compounds that can be employed in the present disclosure, include, but are not limited to, trimethylaluminum, triethylaluminum, and tributylaluminum. The organoaluminum precursor can be introduced in the reactor chamber of the MOCVD apparatus neat, or it can be admixed with an inert carrier gas. The prealuminization step is typically performed at a temperature of 450° C. or greater. In one embodiment, the introducing of the organoaluminum precursor typically occurs at a temperature from 500° C. to 600° C. In another embodiment, the introduction of the organoaluminum precursor occurs at a temperature from 600° C. to 900° C. Notwithstanding the temperature in which the organoaluminum precursor is introduced into the reactor chamber, the prealuminization is performed for a time period of 5 seconds to 120 seconds.

After heating the structure shown in FIG. 4 in hydrogen and performing the above mentioned prealuminization step, a contiguous AlN buffer layer 18 is formed on exposed surfaces of each patterned dielectric material structure 14 and on exposed surfaces (A,B) of the (100) silicon substrate 10. The resultant structure including the contiguous AlN buffer layer 18 is shown, for example, in FIG. 5.

The contiguous AlN buffer layer 18 is formed by introducing an organoaluminum precursor (i.e., a trialkylaluminum compound as mentioned above) and a nitride precursor such as, for example, ammonium nitride into the reactor chamber of the MOCVD apparatus. An inert carrier gas may be present with one of the precursors used in forming the contiguous AlN buffer layer 18, or an inert carrier gas can be present with both the precursors used in forming the contiguous AlN buffer layer 18. The contiguous AlN buffer layer 18 is typically formed at a temperature of 600° C. or greater. In one embodiment, the deposition of the contiguous AlN buffer layer 18 typically occurs at a temperature from 650° C. to 850° C. In another embodiment, the deposition of the contiguous AlN buffer layer 18 typically occurs at a temperature from 850° C. to 1050° C. Notwithstanding the temperature in which the contiguous AlN buffer layer 18 is formed, the deposition of the contiguous AlN buffer layer 18 is performed for a time period of 1 minute to 20 minutes. The contiguous AlN buffer layer 18 that is formed typically has a thickness from 10 nm to 250 nm, with a thickness from 60 nm to 80 nm being even more typical. The Applicant of the present application has found that when the contiguous AlN buffer layer 18 is within the above described ranges, the selectivity and control of dual phase gallium nitride material deposition can be improved when a thicker AlN buffer layer is formed. For example, a 64 nm AlN buffer layer provides higher selectivity and control for dual phase gallium nitride material deposition as compared to a 32 nm AlN buffer layer. The 32 nm AlN buffer layer provides higher selectivity and control for dual phase gallium nitride material deposition as compared to a 10 nm AlN buffer layer.

Referring now to FIG. 6, there is illustrated the structure of FIG. 5 after selectively forming a dual phase gallium nitride material 20 surrounding each sidewall of each patterned dielectric material structure 14 and located adjacent the surface (i.e., surface A) of the silicon substrate having the (111) crystal plane. The dual phase gallium nitride material 20 essentially fills the entirety of each opening; a void 21 can be

present within each opening. As shown in FIG. 6, a bottom-most surface of the dual phase gallium nitride material 20 extends above the planar surface (designated previously as B) of the (100) silicon substrate 10 that has a (100) crystal plane.

In accordance with the present disclosure, the dual phase gallium nitride material 20 comprises a wurtzite phase (designated by the region labeled 22 in the drawings) and a cubic phase (designated by the region labeled 24 in the drawings). The term "wurtzite phase" denotes that the c-direction of the dual phase gallium nitride material 20 is aligned with (111) direction of the original (100) silicon substrate 10. In accordance with an aspect of the present disclosure, the cubic phase 24 of the dual phase gallium nitride material 20 defines at least a portion of an uppermost surface of the dual phase gallium nitride material 20. In some embodiments, an entire uppermost surface of the dual phase gallium nitride material 20 can comprise the cubic phase. In other embodiments, and as shown, a portion of the wurtzite phase 24 can define a remaining portion of the uppermost surface of the dual phase gallium nitride material 20. In some embodiments of the present disclosure, the cubic phase 24 of the dual phase gallium nitride material 20 has a shape of an inverted triangle (see FIG. 6 and the SEM shown in FIG. 7 of the present disclosure). As shown, the base of the inverted triangular constitutes an uppermost surface of the dual phase gallium nitride material 20, while the apex of the inverted triangular is located beneath the uppermost surface of the dual phase gallium nitride material.

In accordance with an aspect of the present disclosure, the dual phase gallium nitride material 20, particularly the wurtzite phase 22, nucleates from the AlN buffer layer 18 that is present at the surfaces having the (111) crystal plane within each opening 17. As the two fronts of the gallium nitride material having the wurtzite phase meet, a phase change to cubic occurs. As such, when the two fronts of the gallium nitride having the wurtzite phase travel a short distance before contacting each other, more cubic phase forms and covers more at the uppermost surface of the gallium nitride material. Conversely, when the two fronts of the gallium nitride having the wurtzite phase travel a long distance before contacting each other, less cubic phase forms and covers less at the uppermost surface of the gallium nitride material. The former case is more controlled and uniform than the latter case is.

In some embodiments of the present disclosure, and as illustrated in FIG. 6, a void 21 can be formed within each opening 17. When present, void 21 is formed within a bottommost portion of the region containing the wurtzite phase 22. In other embodiments (not shown), no void is formed. The void 21 may have a tip portion that is in contact with a portion, i.e., the apex portion of the inverted triangle of the cubic phase 24. In some embodiments, the dual phase gallium nitride material 20 may have an uppermost surface that is coplanar with the uppermost surface of each patterned dielectric material structure 14. In other embodiments the dual phase gallium nitride material 20 may have an uppermost surface that is vertically offset, either above or below, the uppermost surface of each patterned dielectric material structure 14.

In one embodiment of the present disclosure, the dual phase gallium nitride material 20 is pure gallium nitride. In another embodiment of the present disclosure, the dual phase gallium nitride material 20 comprises gallium nitride that includes at least one other Group III element such as, for example, Al and/or In. In such an embodiment, the dual phase gallium nitride material 20 may comprise GaAlN, GaInN or GaAlInN. Notwithstanding the composition of the dual phase gallium nitride material 18, the dual phase gallium nitride material 18 is single crystal.

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The deposition of the dual phase gallium nitride material **20** includes introducing an organogallium precursor and a nitride precursor such as, for example, ammonium nitride into the reactor chamber of the MOCVD apparatus. In some embodiments, an optional organoaluminum precursor (such as described above) and/or an optional organoindium precursor (such as, for example, a trialkylindium compound, e.g., trimethylindium) can also be used. Examples of organogallium precursors that can be employed in the present disclosure include trialkylgallium compounds such as, for example, trimethylgallium and triethylgallium. An inert carrier gas may be present with one of the precursors used in forming the dual phase gallium nitride material **20**, or an inert carrier gas can be present with both the precursors used in forming the dual phase gallium nitride material **20**. The deposition of the dual phase gallium nitride material is typically performed at a temperature of 850° C. or greater. In one embodiment, the deposition of the dual phase gallium nitride material **20** typically occurs at a temperature from 900° C. to 1200° C. In another embodiment, the deposition of the dual phase gallium nitride material **20** typically occurs at a temperature from 1200° C. to 1400° C. Notwithstanding the temperature in which the dual phase gallium nitride material **20** is formed, the deposition of the dual phase gallium nitride material **20** is performed for a time period of 1 minute to 2 hours. The dual phase gallium nitride material **20** that is formed typically has a thickness from 100 nm to 5000 nm, with a thickness from 500 nm to 1000 nm being even more typical.

Referring now to FIG. 7, there is illustrated a scanning electron micrograph (SEM) of a structure including a dual phase gallium nitride material integrated on a (100) silicon substrate that is formed using the method of the present disclosure. The SEM clearly depicts that a dual phase GaN material containing a cubic GaN phase and a wurtzite GaN phase (w) was formed using the method of the present disclosure. Independently, transmission electron microscope and X-ray diffraction studies are realized to confirm the dual phase formation and to identify the initiation of wurtzite to cubic phase transition as where the opposite wurtzite growth fronts first meet—that meeting point later becomes the apex of the inverted triangle containing the cubic phase material.

After forming the structure shown in FIG. 6, semiconductor devices such as, for example, field effect transistors (FET), photonic devices (i.e., light emitting diodes or laser diodes) and combinations thereof, can be formed using conventional process that are well known to those skilled in the art. In some embodiments, the semiconductor devices can be formed upon and within the dual phase gallium nitride material **20**. In other embodiments, the semiconductor devices can be formed upon and within the dual phase gallium nitride material **20** and on an epitaxial semiconductor material that can be grown adjacent the dual phase gallium nitride material **20** and on an exposed uppermost surface of the original (100) silicon substrate **10**. When FETs are formed upon and within the dual phase gallium nitride material **20**, a portion of the dual phase gallium nitride material **20** can serve as a device channel and a gate stack including at least a gate dielectric material and gate electrode can be formed above the device channel utilizing conventional silicon complementary metal oxide semiconductor (CMOS)-like processes. In some embodiments, the FETs built atop the dual phase gallium nitride material **20** can be interconnected with existing silicon CMOS circuits to form a hybrid system. Some examples of fabricating semiconductor devices are now described. In some embodiments, a photonic device can be sandwiched between a topmost and bottommost surface of the (100) silicon substrate **10**.

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Reference is first made to the structure shown in FIG. 8 which shows the structure of FIG. 6 after forming semiconductor devices **50** upon and within the dual phase gallium nitride material **20**. In some embodiments, an interconnect **52** can be present above a patterned dielectric material structure **14** that connects one of the semiconductor devices **50** to a neighboring semiconductor device **50**. In this embodiment, the semiconductor devices **50** can be FETs that are formed upon and within the dual phase gallium nitride material **20**, and interconnect **52** can be a conductive material. As shown, some of the semiconductor devices **50** can be formed directly on a portion of the dual phase gallium nitride material **20** that has the cubic phase **24**.

Reference is now made to FIGS. 9-11 which illustrate another embodiment of the present disclosure in which the structure shown in FIG. 6 can be used as a template for forming semiconductor devices thereon. Specifically, FIG. 9 illustrates the structure of FIG. 6 after formation of another dielectric material **54**. The another dielectric material **54** may include one of the dielectric materials mentioned above, or the another dielectric material **54** may include a planarizing dielectric material such as, for example, a photoresist, a silicate glass, or an oxide such as silicon dioxide. As shown, the another dielectric material **54** can be present atop the dual phase gallium nitride material **20** and atop a portion of the contiguous AlN buffer layer **18** that is present on uppermost surfaces of each of the patterned dielectric material structures **14**.

The another dielectric material **54** can be formed by a deposition process including, but not limited to, chemical vapor deposition, plasma chemical vapor deposition, chemical solution deposition, evaporation and spin-on coating. The thickness of the another dielectric material **54** is typically from 100 nm to 10,000 nm, with a thickness from 2000 nm to 4000 nm being more typical for chemical-mechanical polishing purposes. Other thickness can be employed so long as the uppermost surface of the another dielectric material **54** is above a horizontal portion of the contiguous AlN buffer layer **18** that is present on the uppermost surface of each of the patterned dielectric material structures **14**.

Referring now to FIG. 10, there is illustrated the structure of FIG. 9 after performing planarization which removes a portion of the another dielectric material **54** and the horizontal portion of the contiguous AlN buffer layer **18** that is present on uppermost surface of each of the patterned dielectric material structures **14** stopping on an uppermost surface of the dual phase gallium nitride material **20** and an uppermost surface of each patterned dielectric material structure **14**. A planar structure is provided in which remaining portions of the AlN buffer layer **18'**, dual phase gallium nitride material **20**, and each patterned dielectric material structure **14** have uppermost surfaces that are coplanar with each other. The planarization process that is used in the present disclosure may include chemical mechanical polishing and/or grinding.

Referring now to FIG. 11, there is illustrated the structure of FIG. 10 after semiconductor device fabrication. In this embodiment, semiconductor devices **50**, e.g., FETs, and interconnects **52** can be formed on one side of the structure including the exposed dual phase gallium nitride material **20**, photonic devices **53** such as light emitting diodes or laser diodes, and their other contacts can be formed on the opposite side of the structure and on an exposed surface of the original (100) silicon substrate.

Reference is now made to FIGS. 12-15 which illustrate yet another embodiment of the present disclosure in which semiconductor devices can be formed using the structure shown in



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FIG. 6. Specifically, FIG. 12 illustrates the structure of FIG. 6 after removing an uppermost horizontal portion of the contiguous AlN buffer layer 18 that lies atop each patterned dielectric material structure 14. The removal of the uppermost horizontal portion of the contiguous AlN buffer layer 18 that lies atop each patterned dielectric material structure 14 can be performed by planarization. The remaining portion of the AlN buffer layer is labeled as 18'. As shown in the drawing, each of the patterned dielectric material structures 14 is exposed.

Referring now to FIG. 13, there is illustrated the structure of FIG. 12 after removing each patterned dielectric material structure 14 so as to expose a portion of the uppermost surface of the original (100) silicon substrate 10. The removal of each of the exposed patterned dielectric material structure 14 can be performed utilizing an etching process that selectively removes the dielectric material that constitutes the patterned dielectric material structures 14 from the structure. Examples of such an etching process that can be used at this point of the present disclosure include, but are not limited to, hydrofluoric acid.

Referring now to FIG. 14, there is illustrated the structure of FIG. 13 after epitaxially growth of a semiconductor material 56 (the semiconductor material 56 may also be referred to as an epitaxial semiconductor material since it is formed utilizing an epitaxial process) on the exposed portion of the uppermost surface of the (100) silicon substrate 10 and planarization. As shown, sidewall surfaces of the semiconductor material 56 contact pillar portions of the remaining portion of the AlN buffer layer 18', and a bottommost surface of the semiconductor material 56 contacts the uppermost surface of the (100) silicon substrate 10.

Epitaxially growing, epitaxial growth and/or deposition" mean the growth of a semiconductor material on a deposition surface of a semiconductor material, in which the semiconductor material being grown has the same crystalline characteristics as the semiconductor material of the deposition surface. In the present embodiment, the semiconductor material 56 has the same crystalline characteristics as that of the physically exposed uppermost surface of the (100) silicon substrate 10. When the chemical reactants are controlled and the system parameters set correctly, the depositing atoms arrive at the deposition surface with sufficient energy to move around on the surface and orient themselves to the crystal arrangement of the atoms of the deposition surface. Thus, an epitaxial film deposited on a {100} crystal surface will take on a {100} orientation. In some embodiments, the epitaxial deposition process is a selective deposition process.

The semiconductor material 56 that can be epitaxially deposited includes any semiconductor material such as, for example, silicon (Si), germanium (Ge), and silicon germanium (SiGe). In one embodiment, the semiconductor material 56 includes a same semiconductor material as that of the silicon substrate 10. In another embodiment, the semiconductor material 56 includes a different semiconductor material as that of the silicon substrate 10. It is noted that the specific material compositions for the semiconductor material 56 are provided for illustrative purposes only, and are not intended to limit the present disclosure, as any semiconductor material that may be formed using an epitaxial growth process.

A number of different sources may be used for the deposition of semiconductor material 56. In some embodiments, in which the semiconductor material 56 is composed of silicon, the silicon gas source for epitaxial deposition may be selected from the group consisting of hexachlorodisilane ( $\text{Si}_2\text{Cl}_6$ ), tetrachlorosilane ( $\text{SiCl}_4$ ), dichlorosilane ( $\text{Cl}_2\text{SiH}_2$ ), trichlorosilane ( $\text{Cl}_3\text{SiH}$ ), methylsilane ( $(\text{CH}_3)\text{SiH}_3$ ), dimeth-

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ylsilane ( $(\text{CH}_3)_2\text{SiH}_2$ ), ethylsilane ( $(\text{CH}_3\text{CH}_2)\text{SiH}_3$ ), methyl-disilane ( $(\text{CH}_3)_2\text{Si}_2\text{H}_5$ ), dimethyldisilane ( $(\text{CH}_3)_2\text{Si}_2\text{H}_4$ ), hexamethyldisilane ( $(\text{CH}_3)_6\text{Si}_2$ ) and combinations thereof. In some embodiments, in which semiconductor material 56 is composed of germanium, the germanium gas source for epitaxial deposition may be selected from the group consisting of germane ( $\text{GeH}_4$ ), digermane ( $\text{Ge}_2\text{H}_6$ ), halogermane, dichlorogermane, trichlorogermane, tetrachlorogermane and combinations thereof. In some embodiments, in which the semiconductor material 56 is composed of silicon germanium, the silicon sources for epitaxial deposition may be selected from the group consisting of silane, disilane, trisilane, tetrasilane, hexachlorodisilane, tetrachlorosilane, dichlorosilane, trichlorosilane, methylsilane, dimethylsilane, ethylsilane, methyl-disilane, dimethyldisilane, hexamethyldisilane and combinations thereof, and the germanium gas sources may be selected from the group consisting of germane, digermane, halogermane, dichlorogermane, trichlorogermane, tetrachlorogermane and combinations thereof.

The temperature for epitaxial semiconductor deposition typically ranges from 550° C. to 900° C. Although higher temperature typically results in faster deposition, the faster deposition may result in crystal defects and film cracking. The apparatus for performing the epitaxial growth may include a chemical vapor deposition (CVD) apparatus, such as atmospheric pressure CVD (APCVD), low pressure CVD (LPCVD), plasma enhanced CVD (PECVD), metal-organic CVD (MOCVD) and others. The epitaxial semiconductor material 56 that is deposited can be doped or undoped. By "undoped" it is meant that the maximum dopant concentration of p-type or n-type dopants that are present in the epitaxial semiconductor material is less than  $5 \times 10^{17}$  atoms/cm<sup>3</sup>.

Following the epitaxial growth of semiconductor material 56, a planarization process such as chemical mechanical polishing and/or grinding can be used to provide the planar structure shown in FIG. 14.

Referring now to FIG. 15, there is illustrated the structure of FIG. 14 after semiconductor device fabrication. In this embodiment, semiconductor devices 50, e.g., FETs, are formed upon and within both the dual phase gallium nitride material 20 and the semiconductor material 56.

Reference is now made to FIGS. 16-18 which illustrate a further embodiment of the present disclosure which employs the structure shown in FIG. 6 as a template structure for forming semiconductor devices. Specifically, FIG. 16 illustrates the structure of FIG. 13 after removing sidewall portions, i.e., pillar portions, of the remaining AlN buffer layer so as to expose a portion of a sidewall of each gallium nitride material. The removal of the pillar portions of the remaining AlN buffer layer can be performed utilizing an etching process that selectively removes the exposed sidewall portions of the remaining AlN buffer layer. In one embodiment of the present disclosure, the etching process that can be used to selectively remove the exposed sidewall portions of the remaining AlN buffer layer comprises potassium hydroxide (KOH) or sulfuric acid ( $\text{H}_2\text{SO}_4$ ). As shown, a portion of the AlN buffer layer (labeled as 18") remains within each of the openings that were formed into the (100) silicon substrate, and a topmost surface of element 18" is coplanar with an uppermost surface of the original (100) silicon substrate.

Referring now to FIG. 17, there is illustrated the structure of FIG. 16 after epitaxially growth of a semiconductor material 56 on an exposed portion of the uppermost surface of the (100) silicon substrate and planarization. The material of semiconductor material 56, epitaxial growth process, and planarization process used in this embodiment is the same as that mentioned above for forming the structure shown in FIG.

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14. In this embodiment of the present disclosure a gap 55 is present between the semiconductor material 56 and the dual phase gallium nitride material 20.

Referring now to FIG. 18, there is illustrated the structure of FIG. 17 after semiconductor device fabrication. In this embodiment, semiconductor devices 50, e.g., FETs, are formed upon and within both the dual phase gallium nitride material 20 and the semiconductor material 56. An interconnect 52 can be present which can connect semiconductor devices located on the dual phase gallium nitride material to semiconductor devices located on the semiconductor material 56.

Reference is now made to FIGS. 19-22 which illustrate a yet further embodiment of the present disclosure which employs the structure shown in FIG. 6 as a template structure for forming semiconductor devices. Specifically, FIG. 19 illustrates the structure of FIG. 16 after forming a dielectric material liner 58. The dielectric material liner 58 may comprise a dielectric oxide, dielectric nitride, and/or dielectric oxynitride. In one embodiment of the present disclosure, the dielectric material liner 58 comprises silicon dioxide or silicon nitride. The dielectric material liner 58 can be formed utilizing a conformal deposition process such as, for example, chemical vapor deposition, plasma enhanced chemical vapor deposition or atomic layer deposition. By "conformal" it is meant that the deposition provides a film that defines a morphologically uneven interface with another body and has a thickness that is substantially the same (i.e.,  $\pm 10$  Angstroms) everywhere along the interface. The thickness of the dielectric material liner 58 can be from 2 nm to 5 nm, although lesser and greater thicknesses can also be employed.

Referring now to FIG. 20, there is illustrated the structure of FIG. 19 after removing portions of the dielectric material liner 58 and forming dielectric spacers 60. The removal of portions of the dielectric material liner 58 can be performed utilizing an etching process such as, for example, reactive ion etching (RIE). As shown, the portions of the dielectric material liner 58 that are removed are located on horizontal surfaces of the structure shown in FIG. 19.

Referring now FIG. 21, there is illustrated the structure of FIG. 20 after epitaxially growth of a semiconductor material 56 on an exposed portion of the uppermost surface of the (100) silicon substrate and planarization. The material of semiconductor material 56, epitaxial growth process, and planarization process used in this embodiment is the same as that mentioned above for forming the structure shown in FIG. 14.

FIG. 22 is a pictorial representation (through a cross sectional view) illustrating the structure of FIG. 21 after semiconductor device fabrication. In this embodiment, semiconductor devices 50, e.g., FETs, are formed upon and within both the dual phase gallium nitride material 20 and the semiconductor material 56. An interconnect 52 can be present which can connect semiconductor devices located on the dual phase gallium nitride material to semiconductor devices located on the semiconductor material 56.

While the present disclosure has been particularly shown and described with respect to various embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in forms and details may be made without departing from the spirit and scope of the present disclosure. It is therefore intended that the present disclosure not be limited to the exact forms and details described and illustrated, but fall within the scope of the appended claims.

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What is claimed is:

1. A method for selectively forming a dual phase gallium nitride material on a silicon substrate, said method comprising:

forming a blanket layer of dielectric material on an uppermost surface of a (100) silicon substrate;

patterning said blanket layer of dielectric material forming a plurality of patterned dielectric material structures on portions of the uppermost surface of the (100) silicon substrate and exposing other portions of the uppermost surface of the (100) silicon substrate;

etching said exposed other portions of the uppermost surface of the (100) silicon substrate to expose a surface having a (111) crystal plane within the (100) silicon substrate;

forming a contiguous AlN buffer layer on exposed surfaces of each of said patterned dielectric material structures and on exposed surfaces of the silicon substrate; and

forming a dual phase gallium nitride material on a portion of the contiguous AlN buffer layer and surrounding each sidewall of each of said patterned dielectric material structures, wherein said dual phase gallium nitride material comprises a wurtzite phase and a cubic phase, wherein the cubic phase defines at least a portion of an uppermost surface of the gallium nitride material.

2. The method of claim 1, wherein a distance from a sidewall surface of one patterned dielectric material structure to a sidewall surface of a neighboring patterned dielectric material structure is from 200 nm to 500 nm.

3. The method of claim 1, wherein a distance from a sidewall surface of one patterned dielectric material structure to a sidewall surface of a neighboring patterned dielectric material structure is from greater than 500 nm and up to 5000 nm.

4. The method of claim 1, further comprising heating the etched silicon substrate including said plurality of patterned dielectric material structures in an atmosphere of hydrogen and prealuminizing the exposed surfaces of the silicon substrate.

5. The method of claim 1, wherein said forming the contiguous AlN buffer layer comprises introducing an organoaluminum precursor and a nitride precursor and depositing said precursors at a temperature of 600° C. or greater.

6. The method of claim 1, wherein said forming said dual phase gallium nitride material comprises metalorganic chemical vapor deposition (MOCVD), and said MOCVD is performed at a temperature from 850° C. or greater.

7. The method of claim 1, wherein said cubic phase of said dual phase gallium nitride material has a shape of an inverted triangular and wherein a base of said inverted triangular constitutes the entirety of the uppermost surface of the dual phase gallium nitride material.

8. The method of claim 1, further comprising forming at least one semiconductor device upon and within said dual phase gallium nitride material.

9. The method of claim 1, further comprising:  
forming another dielectric material on exposed surfaces of the contiguous AlN buffer layer, exposed surfaces of the dual phase gallium nitride material and exposed surfaces of the (100) silicon substrate;

planarizing the another dielectric material to provide a planar structure in which uppermost surfaces of the dual gallium nitride material, remaining AlN buffer layer, remaining portion of the another dielectric material and the patterned dielectric structures are coplanar with each other; and

forming at least one semiconductor device upon and within said dual phase gallium nitride material.

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10. The method of claim 1, further comprising forming a photonic device via placing contacts on an exposed bottom-most surface of the (100) silicon substrate.

11. The method of claim 1, further comprising:

removing a horizontal portion of said contiguous AlN 5  
buffer layer from atop each of said patterned dielectric material structures, wherein an uppermost surface of each of said patterned dielectric material structures is exposed;

removing each of said patterned dielectric material struc- 10  
tures to expose a portion of the uppermost surface of the (100) silicon substrate;

epitaxially growing a semiconductor material on said 15  
exposed portion of the uppermost surface of the (100) silicon substrate; and

forming semiconductor devices upon and within the dual phase gallium nitride material and upon within said semiconductor material.

12. The method of claim 1, further comprising:

removing a horizontal portion of said contiguous AlN 20  
buffer layer from atop each of said patterned dielectric material structures, wherein an uppermost surface of each of said patterned dielectric material structures is exposed;

removing each of said patterned dielectric material struc- 25  
tures to expose a portion of the uppermost surface of the (100) silicon substrate;

removing exposed portions of a remaining portion of the 30  
contiguous AlN buffer layer exposing a portion of a sidewall surface of said dual phase gallium nitride material;

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epitaxially growing a semiconductor material on said exposed portion of the uppermost surface of the (100) silicon substrate, wherein a gap is present between the semiconductor material and the exposed portion of the sidewall surface of said dual phase gallium nitride material; and

forming semiconductor devices upon and within the dual phase gallium nitride material and upon within said semiconductor material.

13. The method of claim 1, further comprising

removing a horizontal portion of said contiguous AlN  
buffer layer from atop each of said patterned dielectric material structures, wherein an uppermost surface of each of said patterned dielectric material structures is exposed;

removing each of said patterned dielectric material struc-  
tures to expose a portion of the uppermost surface of the (100) silicon substrate;

removing exposed portions of a remaining portion of the contiguous AlN buffer layer exposing a portion of a sidewall surface of said dual phase gallium nitride material;

forming a dielectric spacer on each exposed sidewall surface of said dual phase gallium nitride material;

epitaxially growing a semiconductor material on said exposed portion of the uppermost surface of the (100) silicon substrate; and

forming semiconductor devices upon and within the dual phase gallium nitride material and upon within said semiconductor material.

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