Advanced flexible electronics: challenges and opportunities

Stephen W. Bedell*, Davood Shahrjerdi, Keith Fogel, Paul Lauro, Can Bayram, Bahman Hekmatshoar, Ning Li, John Ott and Devendra Sadana
IBM T. J. Watson Research Center, 1101 Kitchawan Road, Yorktown Heights, NY, USA 10598

ABSTRACT

Thin, lightweight and flexible electronics are being regarded as an important evolutionary step in the development of novel technological products. Interestingly, this trend has emerged in a wide range of industries; from microelectronics to photovoltaics and even solid state lighting. Historically, most attempts to enable flexibility have focused on the introduction of new material systems that, so far, severely compromise the performance compared to state-of-the-art products. The few approaches that do attempt to render contemporary high-performance materials flexible rely on layer transfer techniques that are complicated, expensive and material-specific. In this paper, we review a method of removing surface layers from brittle substrates called Controlled Spalling Technology that allows one to simple peel material or device layers from their host substrate *after* they have been fabricated. This allows one to fabricate high-performance electronic products in a manner of their choosing, and make them flexible afterwards. This technique is simple, inexpensive and largely independent of substrate material or size. We demonstrate the power and generality of Controlled Spalling by application to a number of disparate applications including high-performance integrated circuits, high-efficiency photovoltaics and GaN-based solid state lighting.

Keywords: Flexible circuits, layer transfer, fracture, photovoltaics, gallium nitride

1. INTRODUCTION

The almost unimaginable diversity of electronic products that exist in the market today make it possible to sense, measure, analyze, transmit and store data across a wide range of platforms almost instantaneously. Likewise, continuous innovation and optimization at the material and device level have led to improvements in the performance and efficiency of the components that underpin these products. What nearly all of these diverse products have in common is a rigid, chip-like form factor. Indeed it is this form factor that permits the product-scale integration of disparate technologies. Recently, however, there has been a growing interest in "flexible" electronic devices; the sophistication of which has been improving at a remarkable rate[1-3]. The techniques for fabricating flexible electronic devices fall broadly into two categories; (*i*) introducing new materials that are natively flexible or (*ii*) making conventional devices flexible by substrate thinning. The main challenge associated with (*i*) is that these new materials are technologically immature and generally have lower performance. However, these natively flexible materials have been improving with time. A good example of this is the active matrix organic light emitting diode (AMOLED) display[4] that is currently being introduced in flexible display products. It would seem that (*ii*) would be a more straightforward method for fabricating flexible electronics, however the few techniques that exist are complicated, expensive and usually specific to a given substrate type.

In this paper we will first describe some of the shortcomings of the present layer transfer techniques for fabricating flexible electronic devices. We will then present a simple fracture-based layer transfer method that is applicable to a wide range of high-performance substrate types. Example applications to flexible complementary metal oxide semiconductor (CMOS) circuits, high-efficiency photovoltaics, and GaN-based solid state lighting will then be shown.

1.1 Layer transfer techniques

Several important layer release methods have been developed including Smart-cut[5], Eltran[6], epitaxial layer lift-off[7] (ELO) and their variants. These methods may be used successfully to remove a surface layer from one substrate material (primarily semiconductors) onto another substrate material by bonding thus enabling a variety of applications, such as silicon-on-insulator (SOI) for CMOS, 3D integration, optoelectronic devices, flexible electronics, to name a few. Despite their usefulness, all of these methods have significant shortcomings. Ion-implantation based techniques such as Smart-cut introduce damage in the substrate material that requires subsequent annealing to remove. This limits the applicability

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of this technique to completed devices. Epitaxial growth-based techniques such as Eltran are extremely material-specific; only Si<001> has demonstrated transfer of high-quality films. Additionally, both ion-implant and epitaxial approaches suffer from the need to use expensive and complicated equipment. Epitaxial lift-off has been successfully applied to GaAs-based photovoltaics[8], however such chemical lift-off techniques use dangerous chemicals and large area lift-off is often challenging in practice. In this paper we review a simple, cost-effective process for removing surface layers from essentially any brittle substrate without the previously described shortcomings. This process is called controlled spalling technology[9] (CST) and is performed at room-temperature using inexpensive laboratory equipment. As a result this approach has the advantage that it can be applied at nearly any point in the semiconductor manufacturing process; from ingots, to starting substrates, to completed devices.

1.2 Controlled spalling

An interesting mode of material failure has been observed for decades wherein a layer possessing tensile stress deposited on the surface of a brittle substrate would peel away from the surface and, in doing so, remove a portion of the substrate. This mode of fracture is referred to as substrate spalling and results from the edge load created by the tensile stressor layer giving rise to a mixture of type I stress (opening mode) and type II stress (shear) which guides the crack to an equilibrium depth below the interface. An analytical model of spalling was developed[10,11,12] in the late 1980s which offered a means of predicting critical loading conditions (film stress and thickness values) for which spalling fracture is possible as well as computing the equilibrium crack depth within the substrate. Historically, the primary interest in spalling research has been to understand how to avoid or suppress what is regarded as a mode of material failure. Recently it was demonstrated[13] that substrate spalling could be used as a means for fabricating thin Si substrates by depositing thick screen-printed metal (Al and Ag) pastes and annealing at 900 ºC. The tensile stress in the metal layers was caused by the coefficient of thermal expansion (CTE) mismatch between the metal and the Si, ultimately leading to spontaneous exfoliation of the surface. The high temperature steps, required for creating the necessary stress, and the spontaneous fracture upon cooling, severely limit the usefulness of the above approach. The high temperature prohibits layer spalling of prefabricated devices, and spontaneous fracture almost always leads to other concurrent modes of fracture, such as film cracking.

In controlled spalling[9,14], the entire process takes place at room temperature, and the parasitic modes of fracture such as channel mode fracture or film cracking are suppressed by mechanically guiding a singular fracture front across the substrate. This is accomplished in three steps; (1) deposition of a tensile stressor layer on the surface of the substrate, (2) application of a handle layer that will help initiate and guide the fracture and (3) gently lifting the handle layer to initiate and propagate the fracture front. An illustration of the controlled spalling process is depicted in Figure 1.

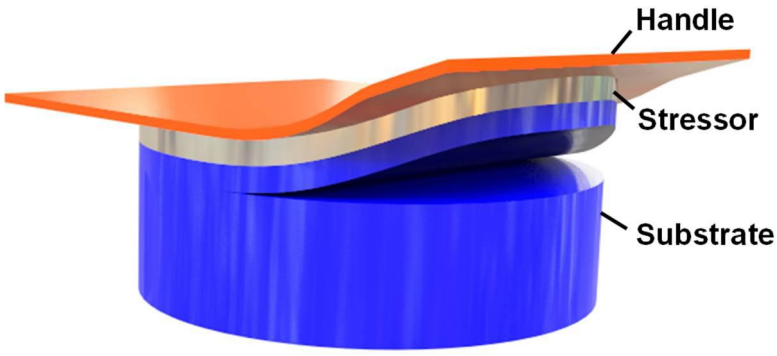

Figure 1. Illustration of the controlled spalling process. A tensile stressor layer is first deposited on the surface of a substrate followed by the application of a flexible handle layer (e.g., tape). By gently lifting the handle layer fracture can be initiated and guided across the substrate. The depth of fracture is mainly determined by the stressor thickness. From Ref. 14 (CC BY 3.0).

1.3 Process window for controlled spalling of Ge(001)

Although theoretically a wide range of materials would work as a stressor, we have found that the high fracture toughness and low deposition cost of Ni make it most suitable for spalling. The role of the stressor layer is to provide sufficient mechanical loading to satisfy the condition for spalling but not enough to cause spontaneous fracture.

Therefore, there exists a continuous range of Ni thickness and stress combinations that will satisfy these conditions and thus define the process window for CST. Figure 2(a) shows data points corresponding to various combinations of Ni stress and thickness that resulted in successful spalling of surface layers from 175μm thick, 100 mm diameter Ge (001) wafers with approximately 4μm Ga(In)As epitaxial surface layers. All these data are from DC magnetron sputtered Ni films and the tensile stress was controlled by adjusting the Ar pressure during deposition. In figure 2(a), wafers that had Ni stress and thickness values in the subcritical region, could not be spalled at all. Therefore, the boundary of this region represents the critical loading condition for spalling of Ge (001) substrates. Wafers with Ni thickness and stress values within the spontaneous region were prone to self-initiated spalling (even during deposition).

Because the depth of fracture is determined mainly by the stressor thickness, the continuous range of Ni thickness in the CST process window permits one to control the thickness of the spalled film. The thickness of the spalled films (fracture depth) was measured and plotted as a function of Ni thickness in Figure 2(b). By using CST, the thickness of the layer can be controlled from roughly 1 to ~100 μm. For thinner layers, the use of buried fracture layers or etch-stop layers have been used in conjunction with CST to remove Si layers at thin as 20 nm from an entire 200 mm diameter bulk Si wafer.

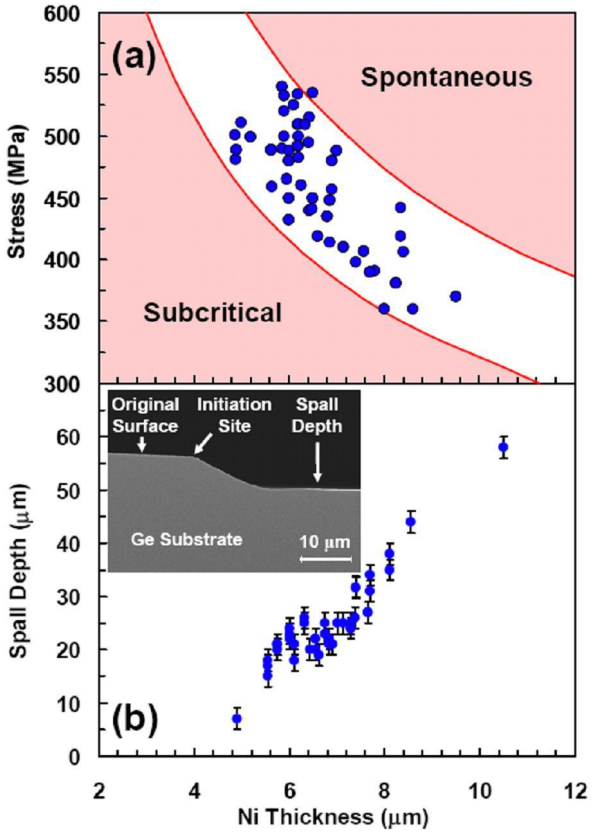

Figure 2. (a) CST process window for Ni stressor layers deposited on Ge (001) substrates. Combinations of Ni stress and thickness in the subcritical region could not be spalled, whereas combinations in the spontaneous region were prone to self-initiated fracture. (b) Measured spalling depth versus Ni thickness for Ge (001) substrates. The inset shows a cross-section SEM image of the fracture initiation site near the edge of the wafer. From Ref. 14 (CC BY 3.0).

One of the most important aspects of CST is the ability to initiate fracture after the stressor layer has been deposited. Although there are many conceivable methods to introduce a crack within a substrate (laser, chemical etch, notching, etc.), the simplest and most reliable method is using stress discontinuity. By forming an abrupt termination of the stressor thickness near the edge of a wafer, very large stress fields can be introduced into the substrate surface. When the handle layer (25 μm thick polyimide tape in this work) is applied over the stressor layer and a small force is exerted near the edge, a crack is formed in the substrate at this high-stress region and propagated using the handle layer. The inset of figure 2(b) shows a cross-section SEM image of the crack-initiation region near the edge of a Ge (001) wafer. The image

shows the original Ge surface, the location of crack initiation (where the free edge of the Ni layer was), and the depth at which fracture occurred (~7μm below the surface).

Although the CST process window described above is for Ge (001), the process steps are similar for all materials, the main difference are the Ni loading conditions depicted in Fig. 2(a) as this is determined by the fracture toughness K_{IC} of the substrate.

2. APPLICATIONS OF CST

2.1 Flexible Si CMOS

The ability to remove surface device layers from substrates at room temperature using only common laboratory equipment makes CST the simplest technique available for rendering rigid circuits flexible. Another useful aspect of CST is that the stressor layer can deposited through a mask making it possible to spall arbitrary shapes. We previously demonstrated[15] successful spalling of state-of-the-art SOI CMOS circuits from 300 mm wafers by depositing a 150 nm Ti / 6 μm Ni stack through a 100 mm diameter shadow mask. The purpose of the Ti layer is to serve both as an adhesion layer, and as etch-stop layer in subsequent processing steps. In principle the entire 300 mm wafer could have been transferred, however, we lacked the necessary equipment for processing the large samples after spalling. Fracture occurred approximately 10 μm below the buried oxide (BOX) / bulk Si interface and in this case a UV-releasable poly vinyl chloride (PVC) based handling tape was used. After spalling, the residual Si layer was etched to the BOX layer using a combination of wet and dry etching. To recover the original Cu-metallized surface, the sample was transferred, BOX-side down, to another layer of handling tape and the original UV-releasable handling tape was removed, and the Ni and Ti layers were removed by wet etching. The process flow is depicted in figure 3(a-d).

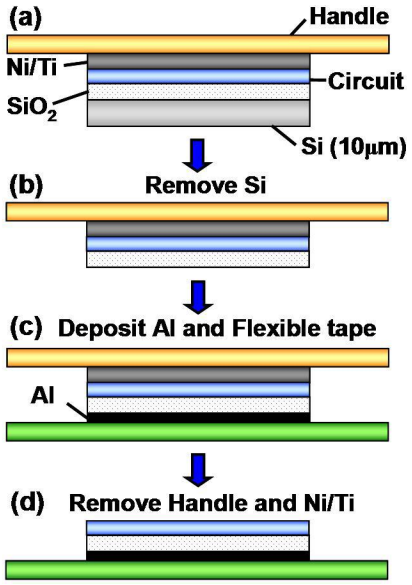

Figure 3. (a) The Si CMOS circuit is removed using the CST process leaving approximately 10 μm residual Si below the BOX layer, which is subsequently removed by etching (b). (c) The back of the circuit is supported using a combination of a thin Al layer and a flexible tape layer permitting the removal of the original handling tape, Ni stressor and Ti adhesion layers (d). From Ref. 14 (CC BY 3.0).

The visual and electrical results are summarized in figure 4(a-c). Figure 4(a) shows completed CMOS circuits fabricated on SOI substrates that have been removed from their host Si wafer using CST. The leftmost circuit in Fig. 4(a) shows the spalled circuit after etching the residual Si back to the BOX layer (*cf*. Fig. 3(b)), whereas the rightmost circuit has been fully processed to recover the original Cu metalized surface (*cf*. Fig. 3(d)). In Fig. 4(b) a cross-section transmission electron microscope (TEM) image is shown of the circuit in 4(a) (leftmost circuit) illustrating the aggressive dimensional scaling and the absence of any spalling-induced damage. Figure 4(c) shows the voltage *vs.* time waveform from a 100

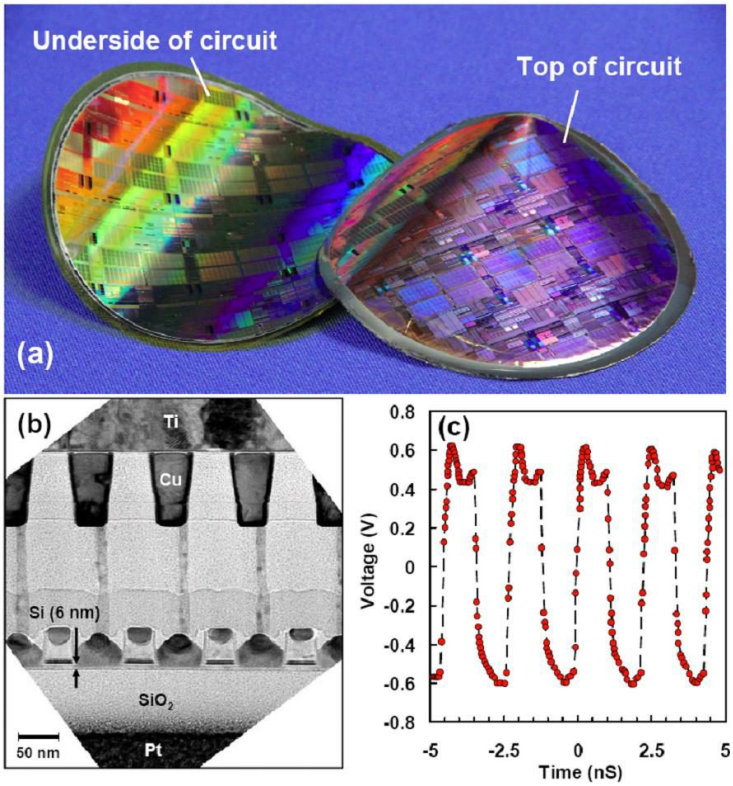

Figure 4. (a) Si CMOS circuit released from the host substrate using the CST process and after removing the residual Si revealing the underside of the circuit (*left*) and after recovering the original Cu surface (*right*). (b) Cross-sectional TEM image of the circuit shown on the left in (a). The Pt layer was deposited during sample preparation. (c) Voltage *versus* time waveform from a 100 stage ring oscillator taken from the flexible circuit shown on the right in (a). From Ref. 14 (CC BY 3.0).

stage ring oscillator taken from the circuit in Fig. 4(a) (rightmost circuit). The 11.4 ps stage delay is similar to the value taken from the circuit prior to spalling and illustrates that the circuit functionality is preserved after the CST process. A more rigorous electrical characterization of these flexible circuits is given elsewhere[15].

2.2 Flexible high-efficiency photovoltaics

In the field of remote power generation, there are many important applications that have strict constraints on area and/or weight. Examples of this include aerospace, military and portable civilian applications. Under these constraints, materials and devices with high photovoltaic conversion efficiency are considered necessary. The preferred devices for these applications are the III-V compound semiconductor multijunction solar cells and methods have existed for decades for making them lightweight and flexible. The two most popular methods are wafer grinding and epitaxial layer lift-off (ELO). The former has the disadvantage that the host substrate, usually GaAs, is lost. Not only are these wafers relatively expensive, but the effluent during the grinding process is toxic. The latter technique, ELO, has the disadvantages that toxic chemicals are used for the process, and the time required to lift-off large-area films is on the order of hours to days. Here we describe the application of CST to the removal of entire 4" wafer dual-junction III-V solar cells grown on Ge (001) substrates[16].

Figure 5(a) shows the process flow used to fabricate these structures. Ni was used as the stressor layer and a 25 μm thick polyimide tape was used as the handle layer. After spalling, all subsequent processing steps were performed with the polyimide handle layer as the carrier. The residual Ge layer (~ 10-15 μm) was removed by dry etching in XeF_2, followed by selective wet etching to the n^+ (In)GaAs contact layer. Cell isolation etching, surface metallization, sintering and anti-reflective coating deposition were then performed to complete device formation. The flexible solar cells demonstrated an efficiency of 28.1% measured under air mass (AM) 1.5 and 1 Sun conditions. This yielded a specific power of nearly 2000 W/kg. Detailed analysis of these flexible devices is given elsewhere[16].

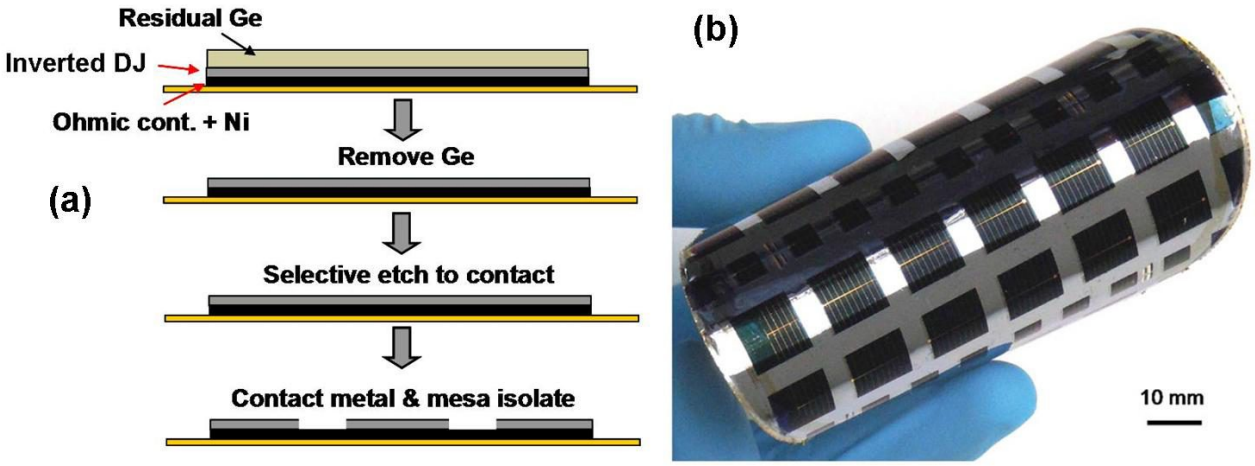

Figure 5. (a) Process sequence used after CST to fabricate high-efficiency, lightweight, flexible solar cells. (b) Image of the flexible dual-junction devices fabricated using this streamlined process. The efficiency of these devices were 28.1% (at 1 Sun) giving a specific power of nearly 2000 W/kg.

2.3 Application to GaN-based materials

The requirement for flexibility is probably less important for solid state lighting than advanced circuitry or remote power generation. However, the weight and cost advantages that CST offers for these expensive materials provides a compelling reason to explore GaN layer transfer; the flexibility, if desired, comes for free.

Until recently, GaN was not available in bulk and was grown on either sapphire or silicon carbide substrates. Although bulk GaN substrates are becoming available, the cost is still prohibitively high for most applications. Due to the high fracture toughness of GaN, the critical loading conditions for Ni differ greatly than that for Ge (001) (Fig. 2(a)). For example, at 400 MPa tensile stress, the critical Ni thickness for Ge spalling is around 6 μm whereas for GaN (on sapphire) it is closer to 20 μm. Because of the greater Ni thickness, electroplating is preferred over sputtering. Typically, a $NiCl_2$ based electroplating chemistry is used which permits plating rates of 1 μm per minute or greater with excellent and consistent mechanical properties. Usually, a thin Ni or Ti/Ni layer is deposited by evaporation or sputtering to act as an electroplating seed layer.

Figure 6(a) shows the process flow used to fabricate spalled light-emitting diode (sLED) devices simply by removing a GaN/InGaN structure from the host sapphire wafer. Figures 6(b) and 6(c) show cross-sectional SEM images of the CST process being used to remove either a portion (~ 1 μm), or the entirety (5 μm) of a GaN/InGaN device layer from a sapphire substrate, respectively. Due to the extreme hardness of sapphire, GaN can be spalled using Ni stress and thickness conditions that make sapphire spalling impossible. Under these conditions fracture can be made to occur at the original GaN/sapphire growth interface resulting in perfect removal of the epitaxial layers from the sapphire surface. Figure 7 shows an example of a 4" GaN/InGaN LED structure removed from a sapphire wafer using this technique and illustrating the high-reflectivity associated with the atomically-resolved fracture. The characteristics of these spalled LED devices (sLED) can be found elsewhere[17].

The recent availability of bulk GaN substrates has allowed manufacturers to fabricate devices (LED and power transistors) on material with 2 to 3 orders of magnitude lower defect density. Unfortunately, the high cost of these substrates limit their use to specialty GaN applications. We have successfully applied the CST process to bulk GaN wafers thereby demonstrating a pathway for GaN substrate reuse and cost reduction. Figure 8 shows a tilt-view SEM image of a ~ 25 μm thick GaN layer that has been removed from a bulk GaN wafer using the CST process.

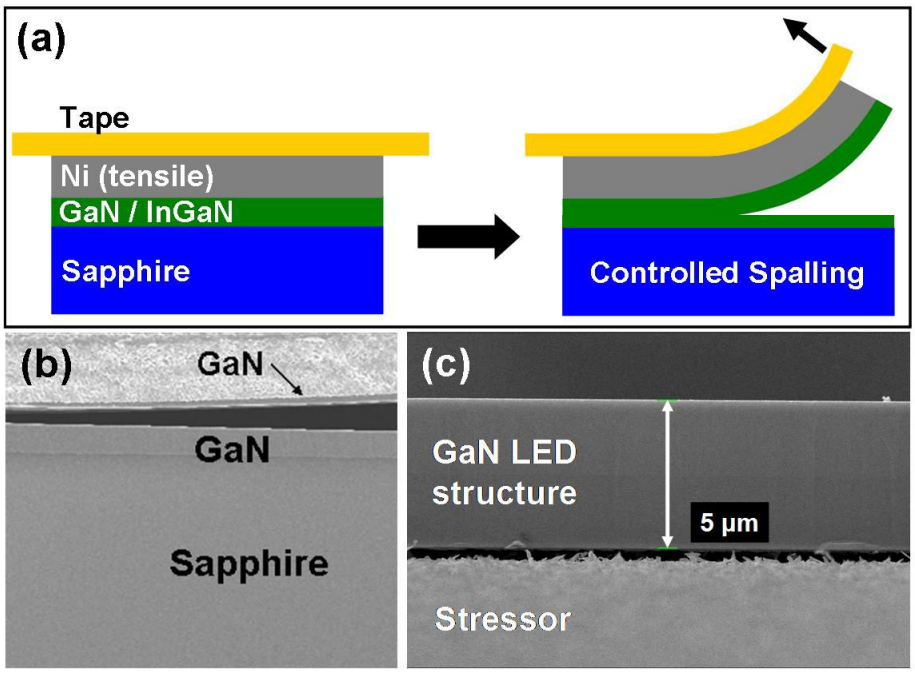

Figure 6. (a) Illustration of the CST process used to remove GaN layers from sapphire substrates. Cross-section SEM images of (b) a thin (~1 µm) and (c) 5 µm thick GaN layer being removed from 4" sapphire substrates.

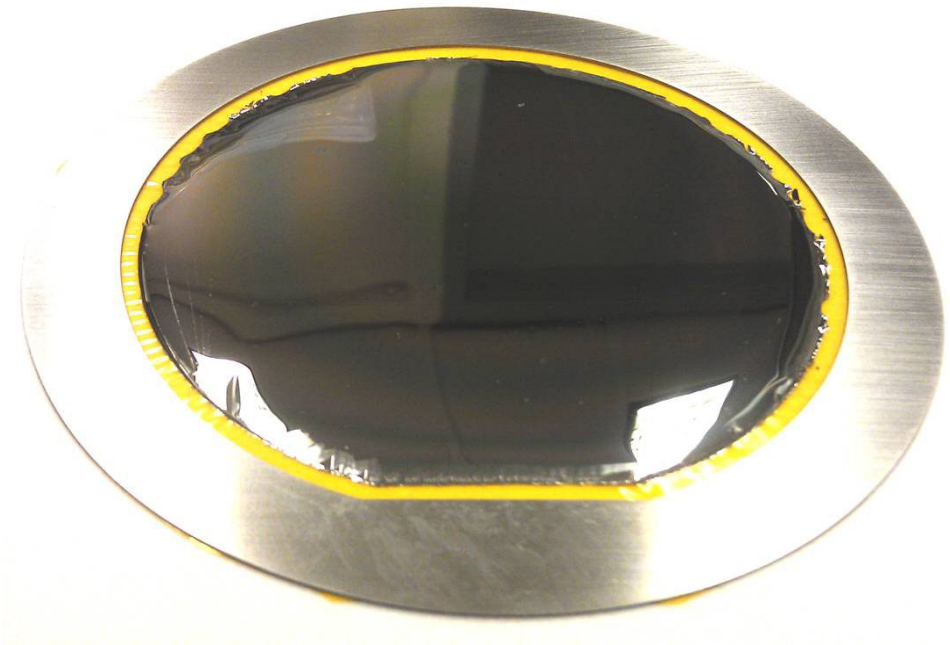

Figure 7. Atomically smooth as-fractured 4" GaN/InGaN LED epitaxial structure separated along the sapphire/GaN growth interface using CST. The reflection of the ceiling can be seen in the surface.

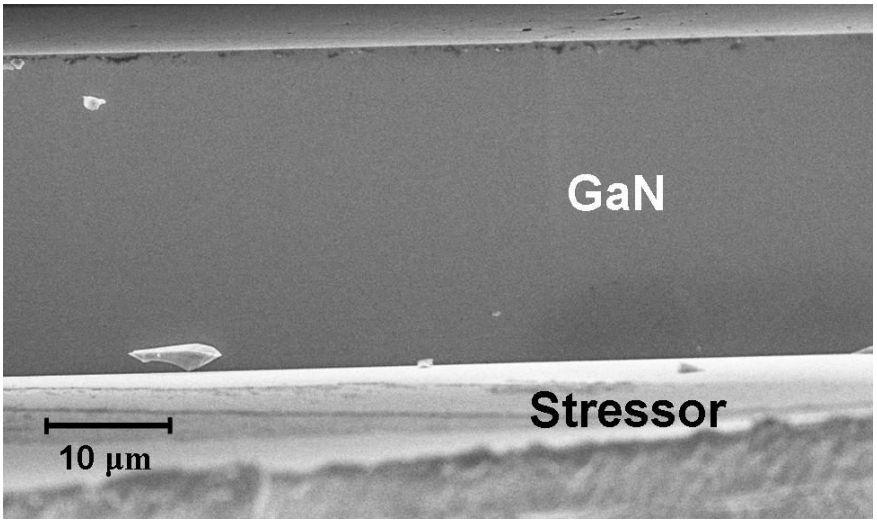

Figure 8. Tilt-view SEM image of a ~ 25 μm thick GaN layer that has been removed from a bulk GaN substrate using the CST process.

3. DISCUSSION AND CONCLUSIONS

Although a wide variety of techniques exist for removing or thinning substrates to enable the fabrication of flexible electronic devices using high-performance materials, none of these are as general or simple as CST. Therefore, we feel that CST is a breakthrough layer transfer technique that eliminates the barrier between flexibility and performance. As with all techniques, there are limitations inherent to CST. For example, because spalling mode fracture works by transferring shear stress down to the crack tip through the overlying material stack, anything that compromises this can cause potential problems. Layered materials that contain a mechanically weak, or poorly adhered, layer will often delaminate at that location rather than at the equilibrium fracture depth (where mode II stress is zero). Also, handling layers that are thick or have high elastic modulus oppose the transference of shear stress to the crack tip (by not letting the Ni compress) and, as a result, the fracture becomes shallower, or is totally arrested in the extreme case. Finally, layered structures that contain materials that yield easily (like low yield stress metals) can effectively arrest the spalling process. In addition to the basic limitations listed above, some material limitations have been observed as well. For instance, although the elemental semiconductors (Ge and Si) can be spalled smoothly with any crystalline orientation, compound semiconductors with a large polar component tend to have very rough surfaces when the fracture path is not coincident with the material fracture planes (usually [110]). Despite these limitations, CST has been successfully applied to Ge, Si, GaAs, InP, GaN and AlN. In all cases, the basic process flow remains the same and only common laboratory equipment is used. In fact, the entire circuit spalling process described in section 2.1 was conducted in a general-purpose laboratory – no cleanroom was necessary.

It would seem that the benefit of using of high-performance CMOS circuits for flexible applications lies in the density of the circuitry, rather than the raw computational power. Another, often neglected, role of the existing rigid form factor is related to the aggressive heat-sinking strategies required for modern high-performance CMOS circuits. Without this aggressive heat-sinking, the computational power of modern circuitry would drop considerably. In fact, even the stand-by power in high-performance CMOS is probably too high[18] for flexible applications with limited cooling. Like most other applications, a Si CMOS technology platform will have to be designed from the bottom-up for use in flexible circuits.

In this paper, we described a method of removing surface layers from brittle substrates called Controlled Spalling Technology that allows one to simple peel material or device layers from their host substrate after they have been fabricated. This allows one to fabricate high-performance electronic products in a manner of their choosing, and make them flexible afterwards. This technique is simple, inexpensive and largely independent of substrate material or size. The generality of Controlled Spalling was illustrated by application to a number of disparate applications including high-performance integrated circuits, high-efficiency photovoltaics and GaN-based solid state lighting.

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