GaN nanostructured *p-i-n* photodiodes

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We report the fabrication of nanostructured *p-i-n* photodiodes based on GaN. Each device comprises arrays of ~200 nm diameter and 520 nm tall nanopillars on a 1 μm period, fabricated by e-beam lithography. Strong rectifying behavior was obtained with an average reverse current per nanopillar of 5 fA at −5 V. In contrast to conventional GaN diodes, nanostructured devices reproducibly show ideality factors lower than 2. Enhanced tunneling through sidewall surface states is proposed as the responsible mechanism for this behavior. Under backillumination, the quantum efficiency in nanostructured devices is partly limited by the collection efficiency of holes into the nanopillars. © *2008 American Institute of Physics*. [DOI: 10.1063/1.3041641]

The available methods for semiconductor nanofabrication allow optoelectronic device designers to rely on nanostructures to improve device performance. A very promising nanostructure to be incorporated in device optimization is the nanopillar, i.e., elongated structure with sidewalls defined by e-beam lithography and dry etching (top-down approach),[1] by direct epitaxial growth with low lateral diffusivity[2] or by self-assembling techniques (bottom-up approaches).[3] In this structure, quantum confinement effects in the lateral direction are only revealed when the lateral dimensions are lower than 50 nm.[1] For larger mesoscopic systems, quantum effects are not observable but the sidewall surface states also make their performance deviate from that found in conventional devices.[4] In particular, light-matter interaction and carrier transport are severely affected in these mesoscopic systems.

The development of III-nitride materials has made possible the fabrication of high-efficiency blue, purple, and ultraviolet (UV) light emitters and UV photodiodes. Recently, nanopatterned III-nitride samples have exhibited enhanced luminescence due to the extraction of guided modes from nanopillar arrays.[5] In this work, we present the fabrication of GaN nanostructured *p-i-n* photodiodes realized via e-beam lithography, and we investigate the effects of the sidewall surface states on their current-voltage (*I-V*) characteristics in darkness and under illumination by comparing the *I-V* characteristics of conventional and nanostructured *p-i-n* photodiodes.

Samples were grown by metal-organic chemical-vapor deposition on transparent AlN templates on double side polished *c*-plane sapphire substrates for backillumination. The structure consisted of a *p-i-n* GaN junction with carrier concentrations of $(5-10)\times 10^{17}$ cm^{-3} for the *p*-type GaN:Mg layer and $(3-5)\times 10^{18}$ cm^{-3} for the *n*-type GaN:Si layer; the *i*-region consisted of an unintentionally doped GaN layer with a residual electron concentration in the 10^{16} cm^{-3} range. In order to minimize the leakage current, the thicknesses of the *p*-type, intrinsic, and *n*-type layers were adjusted to be 285, 200, and 200 nm, respectively.[6]

For nanopillar fabrication, samples were coated with polymethylmethacrylate (PMMA) and soft baked. Lithography was performed using a Leica LV-1 electron-beam system. A 6×4 mm^2 dot field was patterned in the PMMA with a period of 1 μm. To work in the submicron range with sizes beyond the quantum confinement regime, e-beam focus and dose were adjusted to obtain a dot size of approximately 100 nm. After exposure, the PMMA resist was developed and a metal mask consisting of a 720 Å thick Ni layer was deposited using electron-beam evaporation and a lift-off procedure. The pattern was then transferred into the GaN layer to form nanopillars via dry etching in a ECR-RIE system using a $SiCl_4$:Ar plasma etch process. Scanning electron microscopy (SEM) revealed that the etch depth was 520 nm and the resulting nanopillar diameter was about 200 nm, resulting in a 1% fill factor. The sidewall angle was 23°.

Insulating polyimide was spin applied to the sample and cured, covering the nanostructured surface with 1.9 μm thick layer. Oxygen plasma was then used to etch back the polyimide and reveal the top ~100 nm of the nanopillars. SEM analysis of the etched GaN nanopillars after polyimide deposition and etch back shows optimum filling of the space among nanopillars [Fig. 1(a)]. Standard lithography was then used to define broad area circular contacts on the nanostructured surface with 625, 2025, and 3025 μm^2 areas; Ni/Au (400/1200 Å) top contacts were formed by e-beam evaporation and subsequent lift-off. The polyimide in the areas that surround these contacts was then completely removed by using oxygen plasma to allow for deposition of a Ti/Au (400/1200 Å) bottom contact using standard lithography, e-beam evaporation, and lift-off. Figure 1(b) illustrates the schematic of the device after processing. For comparison purposes, conventional devices were also fabricated on the same wafer, following the procedure described elsewhere.[6]

I-V measurements were performed using an HP4155A semiconductor parameter analyzer and a probe station. Ten devices were measured for each of the different active areas and their characteristics were averaged. The resulting curves for the nanostructured diodes show strong rectifying behavior with about seven-orders-of-magnitude contrast between the current levels at 5 and −5 V [Fig. 2(a)]. Unlike conventional diodes, which have currents under the noise floor of the system, increasing leakage currents with reverse bias are observed in the picoampere range. In addition, reverse leakage current increases with increasing diode areas. One poten-

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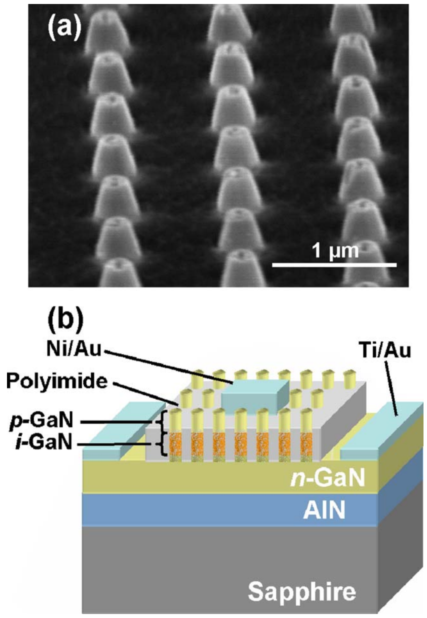

FIG. 1. (Color online) (a) SEM image of the nanopillar array after polyimide deposition and etch back. (b) Schematic of the device.

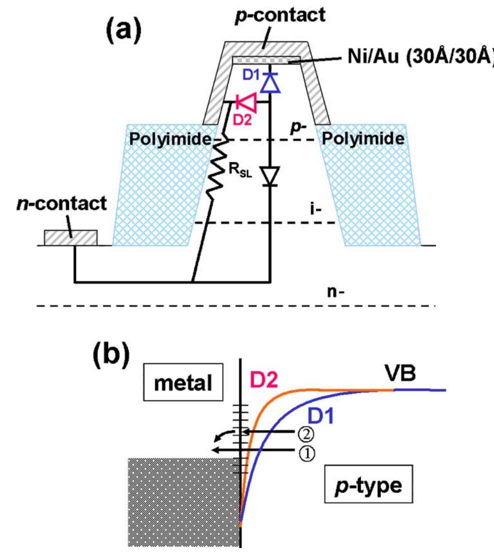

FIG. 3. (Color online) (a) Nanopillar cross section and schematics of the proposed model. (b) Valence band bending at the top (D1) surface of the nanopillar and sidewalls (D2) in the *p*-GaN region and proposed tunneling mechanisms.

tial source of leakage might be the polyimide layer but the undetectable current level observed in reference thin polyimide layers confirms the good insulating properties of the polyimide. On the other hand, part of the leakage current observed in *p*-*n* diodes at low voltages has been previously attributed to the damage induced by the dry etching on the sidewalls of the mesa structures.[7] As nanostructured devices have a much larger sidewall-to-area ratio than conventional devices and the passivating role of the polyimide is uncertain, the reverse bias current might be enhanced by the effect of the surface leakage through the nanopillar sidewalls. This would also explain the increase in the leakage current with increasing diode area, i.e., increasing number of nanopillars under the contact.

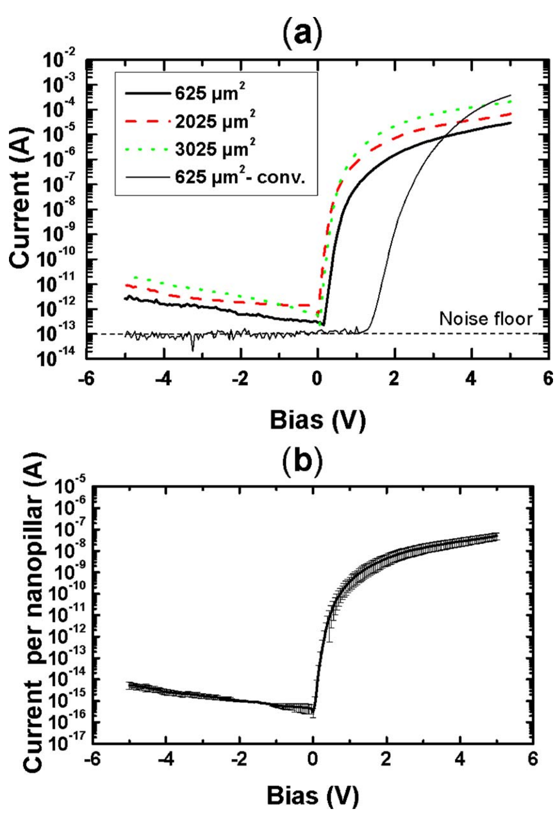

FIG. 2. (Color online) (a) Current-voltage characteristics of GaN nanostructured *p*-*i*-*n* diodes with different device areas (625, 2025, and 3025 μm^2) as compared to 625 μm^2 conventional diodes. (b) Average current-voltage characteristic per nanopillar and error bars (standard deviation) obtained from the measurement of 30 diodes.

Taking into account that the separation between nanopillars is 1 μm, the current per nanopillar can be calculated by dividing the total current by the area of the device. Thus, the average leakage current per nanopillar obtained at −5 V is 5 ± 2 fA [Fig. 2(b)], which corresponds with a current density of 16 ± 6 $\mu A/cm^2$.

A considerable reduction in the turn-on voltage in the nanostructured diodes is also noticeable. Furthermore, the ideality factor obtained from the fitting of the *I*-*V* curves under low forward biases decreases from 2.5–3.0, in the conventional diodes, to 1.3–1.6, in the nanostructured diodes. The former are in good agreement with previous studies on GaN homojunction *p*-*i*-*n* diodes and have been attributed to the downward band bending in the *p*-GaN surface.[8,9] However, the improvement of the ideality factor as well as the reduction in the turn-on voltage in the nanostructured devices are unexpected. One explanation is that, as the top contact covers the surface of the nanopillar and part of the sidewall, the scenario for the *p*-contact formation is different from that in conventional devices. The $SiCl_4$-based etching used to fabricate the nanopillars increases the *n*-type character of the material near the surface.[10] Thus, a highly doped thin layer formed at the sidewalls during etching could raise the electron tunneling current [mechanism 1 in Fig. 3(b)], minimizing the effect of the surface band bending. Moreover, the increase in the surface deep levels as a result of the etching could also benefit trap-assisted tunneling [mechanism 2 in Fig. 3(b)]. In fact, Cl-based dry-etching recipes have demonstrated capabilities to alter the surface properties of GaN layers, improving the ohmicity of *p*-type contacts.[11]

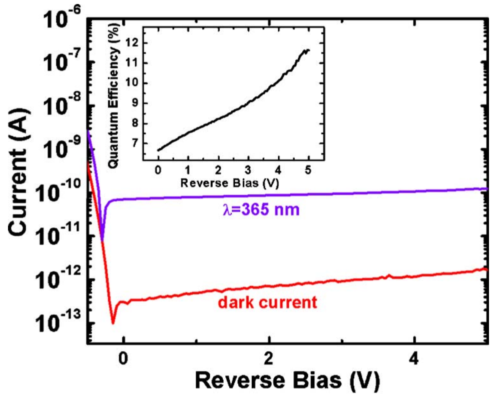

FIG. 4. (Color online) Reverse current of a 625 μm^2 diode in darkness and under back-side illumination at 365 nm. Inset: calculated QE as a function of bias.

The proposed model is presented in Fig. 3. The resistance R_{SL} represents the effect of the surface leakage, whereas D1 and D2 represent the metal-semiconductor barriers at the nanopillar top surface and sidewalls, respectively. The prominent band bending in D2 enhances tunneling, reducing the contact resistance and contributing to improve the ideality factor. However, these effects do not translate into overall higher current in the nanostructured devices under high forward biases (>3 V) due to the lower conduction volume (fill factor $\ll 1$). Consequently, this current is very sensitive to the contact area [Fig. 2(a)].

Photocurrent measurements under backillumination were performed at 365 nm using a Xe lamp and a monochromator (Fig. 4). In this configuration, the light is absorbed in GaN after passing through the sapphire substrate and the AlN buffer layer with minimal losses. As shown in the inset of Fig. 4, the optical response increased significantly with reverse bias: a quantum efficiency (QE) of 6.6% was calculated at 0 V, increasing up to 11.6% at −5 V. On the other hand, the QE of the conventional diodes was about 28% at 0 V and increased up to 30% at 5 V. The QE increase in the conventional devices is attributed to the additional broadening of the depletion region. However, despite experiencing the same depletion region broadening, efficiency increases 2.5 times faster between 0 and −5 V in nanostructured diodes than in conventional diodes.

Two loss mechanisms can account for the reduction in QE in nanostructured diodes: surface recombination[12] and the existence of dead layers due to a low collection efficiency of holes from the *n*-GaN layer into the nanopillar volume. Assuming that surface recombination rate is fairly insensitive to the bias voltage, the faster increase in the photocurrent with bias in nanostructured devices compared to conventional diodes seems to confirm the lateral collection efficiency as a limiting factor. Therefore, we can expect a higher response if we reduce the separation between nanopillars, which provides better lateral collection efficiency in addition to increasing the fill factor. In fact, the distance between nanopillars in our case is about 800 nm, which is still slightly higher than most of the hole diffusion lengths reported in *n*-type GaN.[13,14]

In summary, the fabrication of GaN *p-i-n* photodiodes with embedded nanopillars is reported. Their *I-V* characteristics show an improvement of the ideality factor compared to conventional diodes fabricated on the same material. The enhanced tunneling current through the *p*-type barrier contact is believed to be responsible for this behavior. QEs were found to start lower, but increase faster with reverse bias, as compared to conventional diodes, due to an increasing collection efficiency of minority carriers into the nanopillar.

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